R3210
Data Sheet
32 BIT RISC MICRO PROCESSOR

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Revision History

Rev.	Date	History
1.0	2007 / 01 / 31	Modify 11.3.2 NB Register 42- 43 h description.
1.1	2007/09/05	Modify 2.0 features
1.2	2007/12/19	Modify 14.2 parameter description
1.3	2008/08/28	Modify Master DMA Command/Request Register

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1. Overview

The R3210 is a high performance and fully static 32-bit RISC processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 16KB write direct map L1 cache, PCI rev. 2.1 32-bit bus interface at 33 MHz, SDRAM/ROM/memory controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet MAC, FIFO UART, 10/100M MAC and USB2.0 Host within a single 216-pin LQFP package to form a system-on-a-chip (SOC). It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

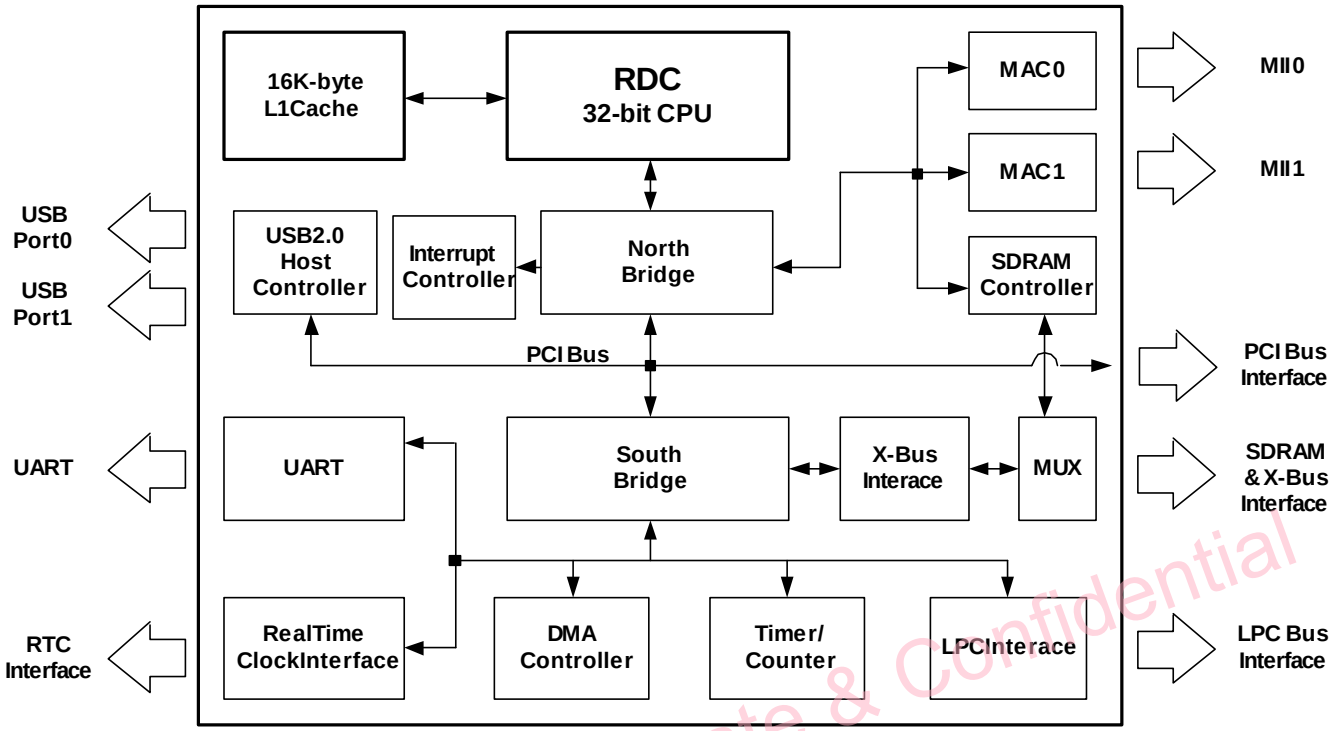
2. Features

- ***Embedded RISC Controller***
  - Full 32-bit RISC architecture
  - Supports diverse operation systems, including Windows based, Linux and most popular 32-bit RTOS
  - 6-stage pipeline
  - Operation frequency: 133 MHz
  - Supports MMU function which includes 32 TLB entries
- ***On-Chip L1 16KB Cache***
  - Unifies instructions and data cache
  - Supports write through for cache write policy
  - Snooping mechanism support for data coherence between main memory and cache
  - Direct map
- ***SDRAM Control Interface***
  - PC100/PC133 compliant
  - Supports 16-bit data bus width
  - Supports speeds up to 133 MHz and above
  - Supports maximum 128Mbyte memory space
- ***X-Bus Interface***
  - Provides the interface to boot ROM BIOS & DOC (Disk On Chip).
  - Supports 8/16-bit data width
  - Provides ROMCS_n for booting from X-bus Flash ROM
  - Supports from 64Kbyte to Max. 16Mbyte ROM space addressing
  - Supports two independent and programmable CSs (Chip Selects)
- ***LPC (Low Pin Count) Bus Interface***
  - LPC revision 1.0 compliant
  - Supports LPC/FWH (Firmware Hub) compliant interfaces
  - Provides the interface to connect an LPC/FWH Flash ROM or Super I/O chip
  - Supports LPC DMA
  - Supports serial IRQ
  - Supports 8/16/32-bit transfer size
  - Supports bus master request in DMA channel 4
- ***MAC Controller***
  - Supports two-port 10/100 Fast Ethernet MAC
  - IEEE 802.3u MII interface
  - IEEE 802.3x flow control in full-duplex mode
  - Descriptor architecture for packet TX/RX
- ***PCI Control Interface***
  - Supports PCI Rev 2.1 specification
  - 32-bit bus interface
  - Supports PCI clock at 33 MHz
  - Supports PCI host
  - Supports PCI master/slave
  - Up to 133 Mbytes/sec maximum bandwidth
  - Supports up to 3 external master devices on PCI
  - Provides four PCI interrupt channels
- ***DMA Controller***
  - Provides two 8237 DMA compatible controllers which are cascaded internally
  - 4 channels for 8-bit DMA transfer and 3

channels for 16-bit transfer

- ***Interrupt Controller***
  - Provides two 8259 compatible interrupt controllers which are cascaded internally
  - Independent programmable level/edge-triggered interrupt channels
  - Serial IRQ supported
- ***Counter/Timers***
  - 8254 compatible timers
  - Provides three independent programmable timers / counters
  - Supports a watchdog timer (WDT)
  - Supports a speaker output
- ***Real Time Clock (External)***
  - Provides a direct interface to external RTC chips
- ***FIFO UART Port***
  - A high performance UART port with transmit and receive FIFOs
  - Supports the programmable baud rate generator with the data rates from 50 to 115,200 bps
  - The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
- ***General Programmable I/O***
  - Supports 58 programmable I/O pins
  - Each GPIO pin can be individually configured to be an input/output pin
- ***Operating Voltage Range***
  - Core voltage: 1.8 V ± 5%
  - I/O voltage: 3.3 V ± 10%
- ***Two USB 2.0 Host Port Support***
  - Supports HS, FS and LS
- ***Package Type***
  - 216-pin LQFP
- ***A Green Product***

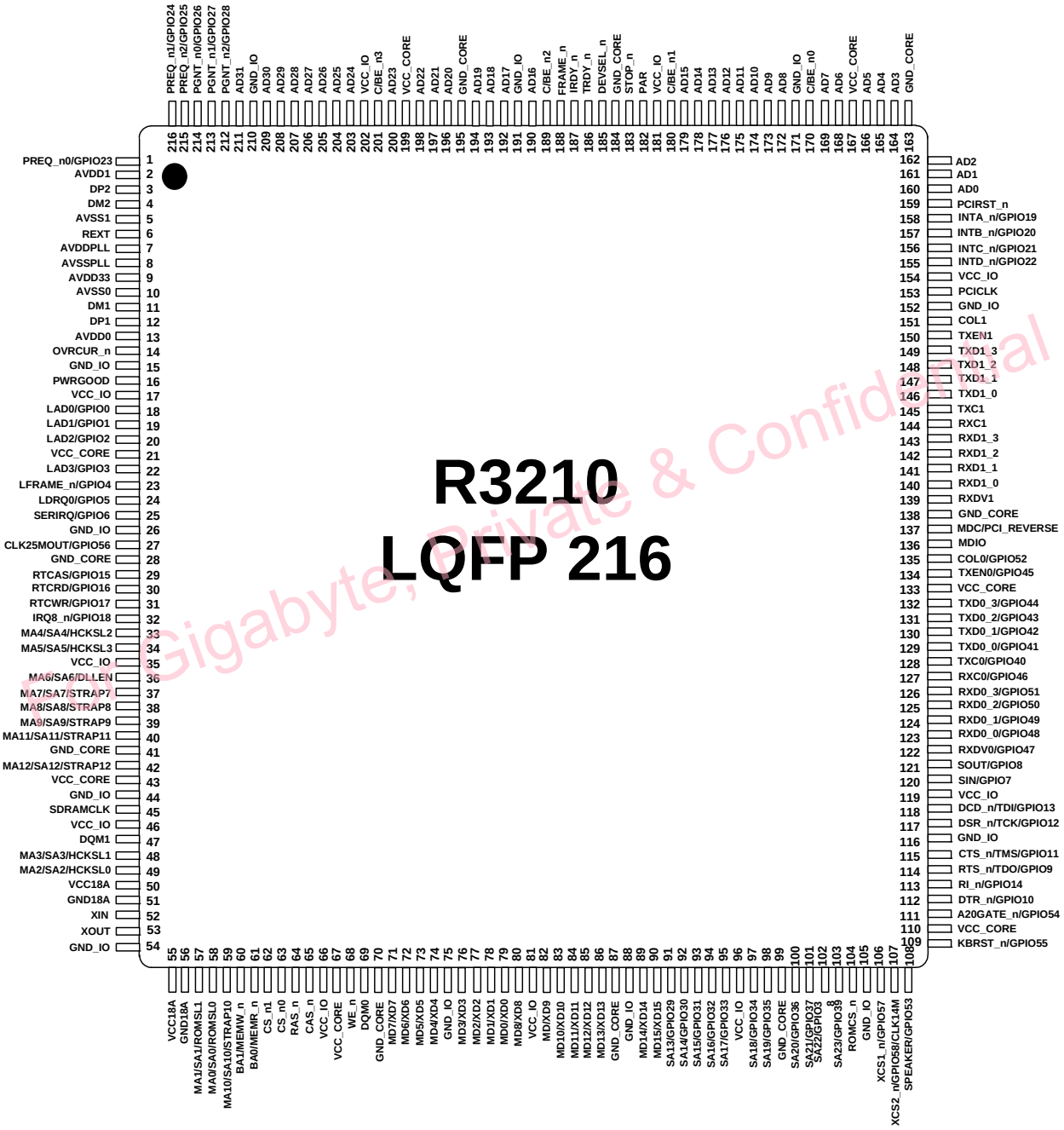
3. Block Diagram



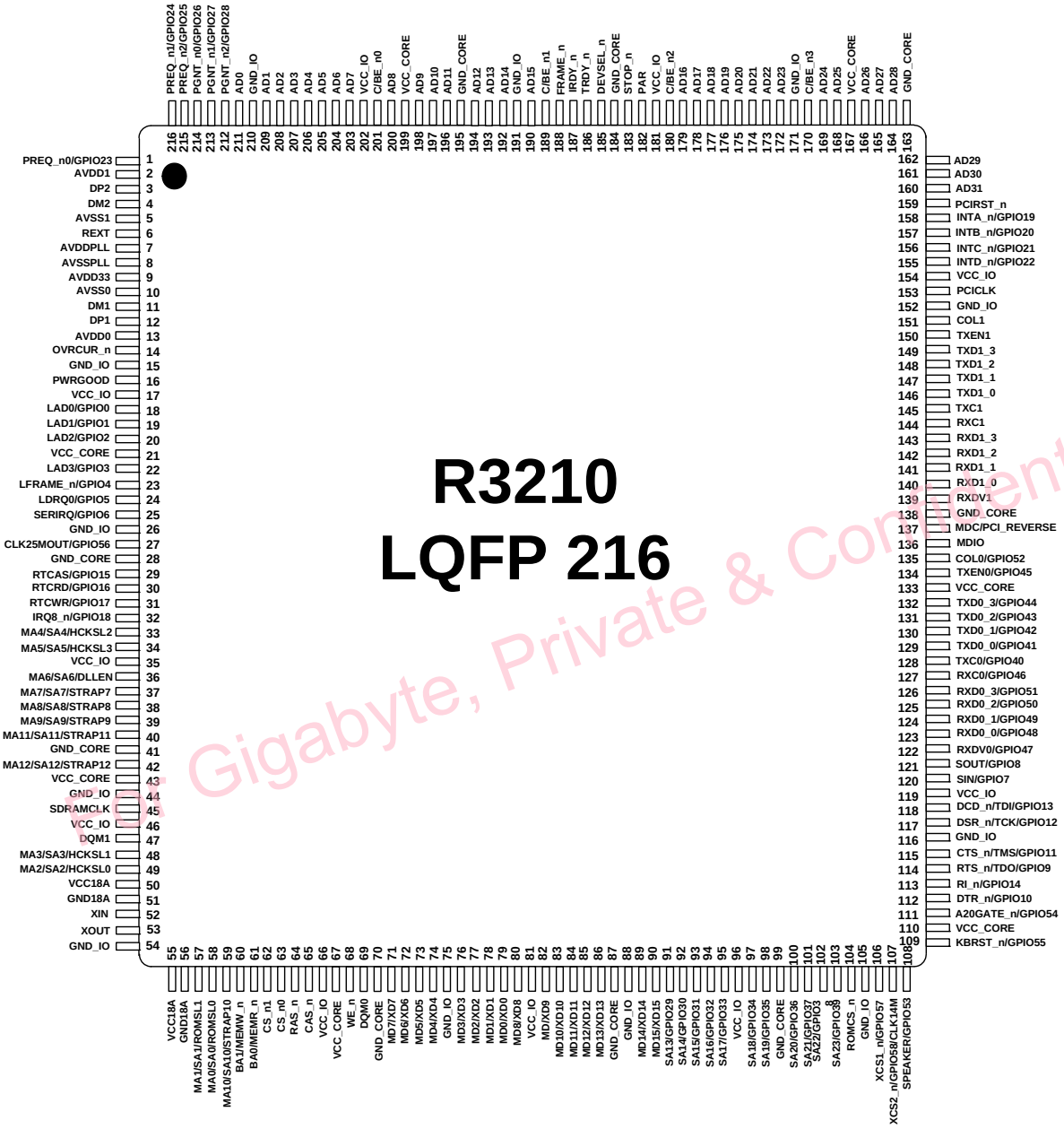
4. PIN Description

4.1 PIN Placement

4.1.1 MDC pulled low



4.1.2 MDC pulled high



4.2 Signal Description

This chapter provides a detailed description of R3210 signals. A signal with the symbol "_n" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin

O Output pin

I/O Bi-directional Input/Output pin

- **System (3 PINs)**

PIN No.	Symbol	Type	Description
16	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The R3210 uses this signal to generate reset sequence for the system.
52	XIN	I	***Crystal-in.*** 25MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
53	XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).

- **PCI Bus Interface (54 PINs)**

PIN No.	Symbol	Type	Description
153	PCICLK	O	***PCI Clock Output.*** This clock is used by all of the R3210 logic that is in the PCI clock domain.
159	PCIRST_n	O	***PCI Reset.*** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
211,209,208,207, 206,205,204,203, 200,198,197,196, 194,193,192,190, 179,178,177,176, 175,174,173,172, 169,168,166,165, 164,162,161,160	AD[31:0]	I/O	***PCI Address and Data.*** The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks. MDC is pulled low: PIN211 is mapped to AD31, PIN 209 to AD30 … MDC is pulled high: PIN211 is mapped to AD0, PIN 209 to AD1 …
201,189,180,170	C/BE_n[3:0]	I/O	***Bus Command and Byte Enables.*** During the address phase, C/BE_n[3:0] define the Bus Command. During the data phase, C/BE[3:0]_n define the Byte Enables. MDC is pulled low: PIN201 is mapped to C/BE_n[3], PIN 189 to C/BE_n[2] … MDC is pulled high: PIN201 is mapped to C/BE_n[0], PIN 189 to C/BE_n[1]…
188	FRAME_n	I/O	***PCI Frame.*** This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.
186	TRDY_n	I/O	***PCI Target Ready.*** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock.
187	IRDY_n	I/O	***PCI Initiator Ready.*** This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock.
183	STOP_n	I/O	***PCI Stop.*** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
185	DEVSEL_n	I/O	***Device Select.*** This pin is driven by the devices which have decoded the addresses belonging to them.
182	PAR	I/O	***PCI Parity.*** This pin is driven to even parity by PCI master over the AD[31:0] and C/BE_n[3:0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.

158	INTA_n/GPIO19	I/O	***PCI INTA_n.*** PCI interrupt input A. It connects to PCI INTA_n when normal modes of PCI Interrupts are supported. ***General-Purpose Input/Output GPIO19.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (INTA_n) is selected.
157	INTB_n/GPIO20	I/O	***PCI INTB_n.*** PCI interrupt input B. It connects to PCI INTNB_n when normal modes of PCI Interrupts are supported. ***General-Purpose Input/Output GPIO20.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (INTB_n) is selected.
156	INTC_n/GPIO21	I/O	***PCI INTC_n.*** PCI interrupt input C. It connects to PCI INTC_n when normal modes of PCI Interrupts are supported. ***General-Purpose Input/Output GPIO21.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (INTC_n) is selected.
155	INTD_n/GPIO22	I/O	***PCI INTD_n.*** PCI interrupt input D. It connects to PCI INTD_n when the normal modes of PCI Interrupts are supported. ***General-Purpose Input/Output GPIO22.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (INTD_n) is selected.
215,216,1	PREQ_n[2:0]/ GPIO25~GPIO23	I/O	***PCI Bus Request.*** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter. ***General-Purpose Input/Output GPIO25~23.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (PREQ_n) is selected.
212,213,214	PGNT_n[2:0]/ GPIO28~GPIO26	I/O	***PCI Grant.*** These signals are the PCI bus grant output signals generated by the internal PCI arbiter. ***General-Purpose Input/Output GPIO28~26.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (PGNT_n) is selected.

- **SDRAM Interface & X Bus (51 PINs)**

PIN No.	Symbol	Type	Description
45	SDRAMCLK	O	***SDRAM Clock output.*** This pin provides the fundamental timing for the SDRAM controller.
57,58	MA[1:0]/SA[1:0]/ ROMSL[1:0]	I/O	***Memory Address MA[1:0].*** These pins are used as the row and column addresses for SDRAM. ***XD Bus Address Bus SA[1:0].*** These pins should be connected to the XD Devices Address Bus SA[1:0]. ***Flash ROM Type Select ROMSL[1:0].*** These two pins are used for system boot strapping options to select the Flash ROM types and physical locations. The logic level of these two pins will be sampled on the rising edge of system reset.

ROMSL1	ROMSL0	Flash ROM Type
0	0	X Bus 8-bit Flash ROM
0	1	LPC Flash ROM
1	0	X Bus 16-bit Flash ROM
1	1	FWH Flash ROM

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>33,48,49</td><td>MA[4:2]/SA[4:2]/
HCKSL[2:0]</td><td>I/O</td><td>Memory Address MA[4:2]. Normally, these pins are used as the row and column addresses for SDRAM.
XD Bus Address Bus SA[4:2]. These pins should be connected to the XD Devices Address Bus SA[4:2].
CPU Clock Selection HCKSL[2:0]. These three pins are used for system boot strapping options to select the Host CPU clock/SDRAM clock which is produced by the PLL based on XIN Clock (25MHz). The logic level of these two pins will be sampled on the rising edge of system reset. The option table is listed as below:
<table><tr><th>HCKSL[2:0]</th><th>CPU Clock</th></tr><tr><td>3’b000</td><td>25MHz</td></tr><tr><td>3’b001</td><td>100MHz</td></tr><tr><td>3’b010</td><td>125MHz</td></tr><tr><td>3’b011</td><td>133MHz</td></tr><tr><td>3’b100</td><td>150MHz</td></tr><tr><td>3’b101</td><td>Reserved</td></tr><tr><td>3’b110</td><td>Reserved</td></tr><tr><td>3’b111</td><td>25MHz (bypass mode)</td></tr></table></td></tr>
<tr><td>34</td><td>MA[5]/SA[5]/
HCKSL[3]</td><td>I/O</td><td>Memory Address MA[5]. Normally, these pins are used as the row and column addresses for SDRAM.
XD Bus Address Bus SA[5]. These pins should be connected to the XD Devices Address Bus SA[3:2].
PCI Clock Selection HCKSL[3]. This pin is used for system boot strapping options to select the PCI clock which is an integer divisor of the SDRAM clock. The logic level of this pin will be sampled on the rising edge of system reset. The option table is listed as below:
<table><tr><th>HCKSL3</th><th>PCI Clock</th></tr><tr><td>0</td><td>CPU Clock/5</td></tr><tr><td>1</td><td>CPU Clock/4</td></tr></table></td></tr>
<tr><td>36</td><td>MA[6]/SA[6]/DLLEN</td><td>I/O</td><td>Memory Address MA6. Normally, this pin is used as the row and column addresses for SDRAM.
XD Bus Address Bus SA6. This pin should be connected to the XD Devices Address Bus SA6.
DeLayLine Enable. This pin is used for system boot strapping option to select enabled or disabled SDRAM clock output Delay Line circuit. It is normaly pulled high to enable the Delay Line. To pull low this pin will bypass the internal Delay Line.</td></tr>
</table>

PIN No.	Symbol	Type	Description
42,40,59,39,38, 37	MA[12:7]/SA[12:7]/ STRAP[12:7]	I/O	***Memory Address MA[12:7].*** Normally, these pins are used as the row and column address for SDRAM. ***XD Bus Address Bus SA[12:7].*** These pins should be connected to the XD Devices Address Bus SA[12:7]. ***STRAP[12:7].*** These pins are used for system boot strapping option. STRAP[7]: Normally, it should be pulled low. Pull it high to enter USB loopback mode. STRAP[8]: Normally, it should be pulled low. Pull it high to select OVRCUR_n pin as USB PLL clock input. STRAP[9]: Normally, it should be pulled low. Pull it high to select SPEAKER pin as PLL test out. STRAP[10]: Normally, it should be pulled low. Pull it high to enable USB PHY parallel data out. STRAP[11]: Normally, it should be pulled low for production. Pull it high to enable R3210 JTAG. STRAP[12]: R3210 timer clock source select. Pull it high to select external 14.318MHz input. Pull it low to select internal 12.5MHz input.
90,89,86,85,84, 83,82,80,71,72, 73,74,76,77,78, 79	MD[15:0]/XD[15:0]	I/O	***Memory Data MD[15:0].*** These pins are connected to the SDRAM data bus. ***XD Data Bus XD[15:0].*** These pins should be connected to the XD Devices Data Bus.
61	BA0/MEMR_n	O	***SDRAM Bank Address.*** These pins are connected to SDRAM as bank address pins. ***XD Bus Memory Read.*** This memory read command signal is used for XD flash ROM read access cycle.
60	BA1/MEMW_n	O	***SDRAM Bank Address.*** These pins are connected to SDRAM as bank address pins. ***XD Bus Memory Write.*** This memory write command signal is used for XD flash ROM write access cycle.
47,69	DQM[1:0]	O	***SDRAM Data Mask DQM[1:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.
62,63	CS_n[1:0]	O	***Chip Select CS[1:0].*** These two pins activate the SDRAM devices. First Bank of SDRAM accepts any command when the CS0_n pin is active low. Second Bank of SDRAM accepts any command when the CS1_n pin is active low.
64	RAS_n	O	***SDRAM Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the SDRAM clock. This signal also allows row access and pre-charge.
65	CAS_n	O	***SDRAM Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the SDRAM clock. This signal also allows column access and pre-charge.
68	WE_n	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.
104	ROMCS_n	O	***ROM Chip Select.*** This pin is used as a ROM chip select.
103,102,101,100, 98,97,95,94,93, 92,91	SA[23:13]/ GPIO39~GPIO29	I/O	***XD Bus Address Bus SA[23:13].*** These pins should be connected to the XD Devices Address Bus SA[23:13]. ***General-Purpose Input/Output GPIO39~29.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (SA[23:13]) is selected.

- **LPC Bus Interface (7 PINs)**

PIN No.	Symbol	Type	Description
22,20,19,18	LAD[3:0]/ GPIO3~GPIO0	I/O	***LPC Command, Address and Data LAD[3:0].*** These pins are used to be command/address/data pins of Low-Pin-Count Function. ***General-Purpose Input/Output GPIO3~GPIO0.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (LAD[3:0]) is selected.

23	LFRAME_n/GPIO4	I/O	***Low Pin Count FRAME_n Signal.*** This signal is used as a frame signal of low pin count protocol. ***General-Purpose Input/Output GPIO4.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (LFRAME_n) is selected.
24	LDRQ_n/GPIO5	I/O	***Low Pin Count DMA Request Signal.*** This signal is used as a DMA request signal of low pin count protocol. ***General-Purpose Input/Output GPIO5.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (LDRQ_n) is selected.
25	SERIRQ/GPIO6	I/O	***Serial Interrupt Request.*** This pin is used to support the serial interrupt protocol of common architecture. ***General-Purpose Input/Output GPIO6.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (SERIRQ) is selected.

Notes:

1. *If these LPC pins are not treated as NC (No Connection) pins, a 10k Ohm external pull-up resistor must be added to each of these LPC pins.*
2. *If these LPC pins are used as NC pins, an external pull-up resistor must be added to LDRQ_n to ensure the system works correctly.*

- **MII Interface (28 PINs)**

PIN No.	Symbol	Type	Description
129,130,131, 132	TXD0_0/GPIO41 TXD0_1/GPIO42 TXD0_2/GPIO43 TXD0_3/GPIO44	I/O	***TXD0_[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal. ***General-Purpose Input/Output GPIO44~GPIO41.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (TXD0_[3:0]) is selected.
128	TXC0/GPIO40	I/O	***TXC0:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active. ***General-Purpose Input/Output GPIO40.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (TXC0) is selected.
127	RXC0/GPIO46	I/O	***RXC0:*** Supports the receive clock supplied by the external PMD device. This clock should always be active. ***General-Purpose Input/Output GPIO46.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RXC0) is selected.
122	RXDV0/GPIO47	I/O	***RXDV0:*** Data valid is asserted by an external PHY when the received data is present on the RXD[3:0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal. ***General-Purpose Input/Output GPIO47.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RXDV0) is selected.
123,124,125, 126	RXD0_0/GPIO48 RXD0_1/GPIO49 RXD0_2/GPIO50 RXD0_3/GPIO51	I/O	***RXD0_[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal. ***General-Purpose Input/Output GPIO51~GPIO48.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RXD0_[3:0]) is selected.
135	COL0/GPIO52	I/O	***COL0:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin. ***General-Purpose Input/Output GPIO52.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (COL0) is selected.
134	TXEN0/GPIO45	I/O	***TXEN0:*** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port. ***General-Purpose Input/Output GPIO45.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (TXEN0) is selected.
146,147,148, 149	TXD1_0 TXD1_1 TXD1_2 TXD1_3	O	***TXD1_[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
150	TXEN1	I/O	***TXEN1:*** This pin functions as Transmit Enable. It indicates that a transmission is active on the MII port to an external PHY device. For internal USB test mode, it is treated as an input.

145	TXC1	I	***TXC1:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
144	RXC1	I	***RXC1:*** Supports the receive clock supplied by the external PMD device. This clock should always be active.
140,141,142, 143	RXD1_0 RXD1_1 RXD1_2 RXD1_3	I/O	***RXD1_[3:0]:*** Four parallel receive data lines. This data is driven by an external PHY that the media is attached and should be synchronized with the RXC signal. For internal USB test mode, it is treated as an output
139	RXDV1	I/O	***RXDV1:*** Data valid is asserted by an external PHY when the received data is present on the RXD1_[3:0] lines and is de-asserted at the end of the packet. For internal USB test mode, it is treated as an output
151	COL1	I/O	***COL1:*** This pin functions as Collision Detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin. For internal USB test mode, it is treated as output
137	MDC/PCI_REVERSE	I/O	***MDC:*** MII management data clock is sourced by the R3210 to the external PHY devices as a timing reference for the transfer of information on the MDIO signal. ***PCI_REVERSE:*** This pin is used for system boot strapping option to select pin sequence of PCI AD bus and CBE bus. Pull low will use the default sequence; pull high will select the reverse sequence of PCI AD bus and CBE bus, i.e., AD31 ⇔ AD0, AD30 ⇔ AD1, AD0 ⇔ AD31, CBE3 ⇔ CBE0, CBE0 ⇔ CBE3…
136	MDIO	I/O	***MDIO:*** MII management data input/output transfers control information and status between the external PHY and the R3210.

- **FIFO UART (8 PINs)**

PIN No.	Symbol	Type	Description
120	SIN/GPIO7	I/O	***Receive Data.*** FIFO UART receiver serial data input signal. ***General-Purpose Input/Output GPIO7.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (SIN) is selected.
121	SOUT/GPIO8	I/O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port. ***General-Purpose Input/Output GPIO8.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (SOUT) is selected.
114	RTS_n/TDO /GPIO9	I/O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***TDO:*** JTAG Test Data Output pin. ***General-Purpose Input/Output GPIO9.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RTS_n) is selected.
112	DTR_n/GPIO10	I/O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***General-Purpose Input/Output GPIO10.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (DTR_n) is selected

PIN No.	Symbol	Type	Description
115	CTS_n/TMS/GPIO11	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_n.* ***TMS:*** JTAG Test Mode Select pin. ***General-Purpose Input/Output GPIO11.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (CTS_n) is selected
117	DSR_n/TCK/GPIO12	I/O	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_n.* ***TCK:*** JTAG Test Clock Input pin. ***General-Purpose Input/Output GPIO12.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1'. Otherwise, the normal function (DSR_n) is selected.
118	DCD_n/TDI/GPIO13	I/O	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD_n.* ***TDI:*** JTAG Test Data Input pin. ***General-Purpose Input/Output GPIO13.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (DCD_n) is selected
113	RI_n/GPIO14	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). An RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_n.* ***General-Purpose Input/Output GPIO14.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RI_n) is selected

- **External RTC Interface (4 PINs)**

PIN No.	Symbol	Type	Description
29	RTCAS/GPIO15	I/O	***RTC Address Strobe.*** This pin is used as the RTC Address Strobe and should be connected to the RTC. ***General-Purpose Input/Output GPIO15.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O

			Control Register to '1', otherwise the normal function (RTCAS) is selected
30	RTCRD/GPIO16	I/O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC. ***General-Purpose Input/Output GPIO16.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RTCRD) is selected
31	RTCWR/GPIO17	I/O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC. ***General-Purpose Input/Output GPIO17.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (RTCWR) is selected
32	IRQ8_n/GPIO18	I/O	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input. ***General-Purpose Input/Output GPIO18.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (IRQ8_n) is selected

- **USB 2.0 Interface (6 PINs)**

PIN No.	Symbol	Type	Description
6	REXT	I	***External Reference Resistance***. 510Ω±10%
14	OVRCUR_n	I	***Over Current Detect for USB Host Controller.*** This pin is used to monitor USB Power Over Current Status.
12,11	DP1, DM1	I/O	***Universal Serial Bus Port 1.*** These are the serial data pair for USB Port 0.
3,4	DP2, DM2	I/O	***Universal Serial Bus Port 2.*** These are the serial data pair for USB Port 1.

- **Miscellaneous & GPIO (6 PINs)**

PIN No.	Symbol	Type	Description
111	A20GATE_n/ GPIO54	I/O	***Address Bit 20 Mask.*** ***General-Purpose Input/Output GPIO54.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (A20GATE_n) is selected.
109	KBRST_n/ GPIO55	I/O	***Keyboard Reset.*** ***General-Purpose Input/Output GPIO55.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (KBRST_n) is selected.
108	SPEAKER/GPIO53	I/O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker. ***General-Purpose Input/Output GPIO53.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (SPEAKER) is selected.
27	CLK25MOUT/ GPIO56	I/O	***25MHz Clock output.*** ***General-Purpose Input/Output GPIO56.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (CLK25MOUT) is selected.
106	XCS1_n/GPIO57	I/O	***XBUS Chip Select 1*** ***General-Purpose Input/Output GPIO57.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (XCS1_n) is selected.
107	XCS2_n/GPIO58/ CLK14M	I/O	***XBUS Chip Select 2*** ***General-Purpose Input/Output GPIO58.*** The General-Purpose Input/Output function is selected by setting the corresponding bits of General-Purpose I/O Control Register to '1', otherwise the normal function (XCS2_n) is selected. **CLK14M.** External 14.318MHz Clock for timer. The R3210 timer will use this

PIN No.	Symbol	Type	Description
			pin as a clock source when MA[12]/STRAP[12] is pulled high during system reset.

- **Power (49 PINs)**

PIN No.	Symbol	Type	Description
17,35,46,66,81, 96,119,154,181, 202	VCC_IO	I	I/O power pin, pure 3.3V.
15,26,44,54,75, 88,105,116,152, 171,191,210	GND_IO	I	I/O ground pin.
21,43,67,110, 133,167,199	VCC_CORE	I	Core power pin, pure 1.8V.
28,41,70,87,99, 138,163,184, 195	GND_CORE	I	Core ground pin.
50,55	VCC18A	I	PLL power pin, pure 1.8V.
51,56	GND18A	I	PLL ground pin.
9	AVDD33	I	I/O power pin, pure 3.3V.
2,13	AVDD[1:0]	I	Analog power pin, pure 1.8V.
7	AVDDPLL	I	USB PLL power pin, pure 1.8V.
5,10	AVSS[1:0]	I	Analog ground pin.
8	AVSSPLL	I	USB PLL ground pin.

4.3 PIN Capacitance Description

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance		4.8		pF
C_{OUT}	3.3V Output Capacitance		4.8		pF
C_{BID}	3.3V Bi-directional Capacitance		4.8		pF

4.4 PIN Pull-up/Pull-down Description

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
PWRGOOD	I	--	0	0	1	Y	--	
XIN	I	--	--	--	--	--	--	Note6
XOUT	O	--	--	--	--	--	--	Note6
PCICLK	O	--	--	--	--	--	--	Note7
PCIRST_n	O	--	--	--	--	--	--	Note7
AD[31:0]	IO	--	1	0	--	--	--	Note7 & Note8
C/BE_n[3:0]	IO	--	1	0	--	--	--	Note7 & Note8
FRAME_n	IO	--	1	0	--	--	--	Note7 & Note8
TRDY_n	IO	--	1	0	--	--	--	Note7 & Note8
IRDY_n	IO	--	1	0	--	--	--	Note7 & Note8

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
STOP_n	IO	--	1	0	--	--	--	Note7 & Note8
DEVSEL_n	IO	--	1	0	--	--	--	Note7 & Note8
PAR	IO	--	1	0	--	--	--	Note7 & Note8
INTA_n/GPIO19	IO	--	Note4	0	--	--	--	Note7 & Note9
INTB_n/GPIO20	IO	--	Note4	0	--	--	--	Note7 & Note9
INTC_n/GPIO21	IO	--	Note4	0	--	--	--	Note7 & Note9
INTD_n/GPIO22	IO	--	Note4	0	--	--	--	Note7 & Note9
PREQ_n[2:0]/GPIO25~GPIO23	IO	--	Note4	0	--	--	--	Note7 & Note9
PGNT_n[2:0]/GPIO28~GPIO26	IO	--	Note4	0	--	--	--	Note7 & Note9
SDRAMCLK	O	Note1	0	0	0	N	Note2	
MA[1:0]/SA[1:0]/ ROMSL[1:0]	IO	Note1	0	0	0	Y	F	
MA[4:2]/SA[4:2]/ HCKSL[2:0]	IO	Note1	0	0	0	Y	F	
MA[5]/SA[5]/ HCKSL[3]	IO	Note1	0	0	0	Y	F	
MA[6]/SA[6]/DLLEN	IO	Note1	0	0	0	Y	F	
MA[12:7]/SA[12:7]/ STRAP[12:7]	IO	Note1	0	1	0	Y	F	
MD[15:0]/XD[15:0]	IO	Note1	0	0	0	Y	F	
BA0/MEMR_n	O	Note1	--	--	--	Y	Note2	
BA1/MEMW_n	O	Note1	--	--	--	Y	Note2	
DQM[1:0]	O	Note1	--	--	--	N	Note2	
CS_n[1:0]	O	Note1	--	--	--	N	Note2	
RAS_n	O	Note1	--	--	--	N	Note2	
CAS_n	O	Note1	--	--	--	N	Note2	
WE_n	IO	Note1	1	0	0	N	Note2	
ROMCS_n	O	Note3	--	--	--	Y	Note2	
SA[23:13]/ GPIO39~GPIO29	IO	8mA	Note4	0	0	N	F	
LAD[3:0]/GPIO3~GPIO0]	IO	--	Note4	0	--	--	--	Note7
LFRAME_n/GPIO4	IO	--	Note4	0	--	--	--	Note7
LDRQ_n/GPIO5	IO	--	Note4	0	--	--	--	Note7
IRQSER/GPIO6	IO	--	Note4	0	--	--	--	Note7
TXD0_0/GPIO41 TXD0_1/GPIO42 TXD0_2/GPIO43 TXD0_3/GPIO44	IO	12mA	Note4	0	0	Y	S	
TXC0/GPIO40	IO	12mA	Note4	0	0	Y	S	
RXC0/GPIO46	IO	12mA	Note4	0	0	Y	S	
RXDV0/GPIO47	IO	12mA	Note4	0	0	Y	S	
RXD0_0/GPIO48 RXD0_1/GPIO49 RXD0_2/GPIO50 RXD0_3/GPIO51	IO	12mA	Note4	0	0	Y	S	
COL0/GPIO52	IO	12mA	Note4	0	0	Y	S	
TXEN0/GPIO45	IO	12mA	Note4	0	0	Y	S	
TXD1_0 TXD1_1 TXD1_2	O	12mA	--	--	--	Y	S	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
TXD1_3								
TXEN1	IO	12mA	0	0	0	Y	S	
TXC1	I	--	0	0	1	Y	--	
RXC1	I	--	0	0	1	Y	--	
RXD1_0 RXD1_1 RXD1_2 RXD1_3	IO	12mA	0	0	0	Y	S	
RXDV1	IO	12mA	0	0	0	Y	S	
COL1	IO	12mA	0	0	0	Y	S	
MDC/PCI_REVERSE	IO	12mA	0	1	0	Y	S	
MDIO	IO	12mA	0	0	0	Y	S	
SIN/GPIO7	IO	Note3	Note4	0	0	Y	Note5	
SOUT/GPIO8	IO	Note3	Note4	0	0	Y	Note5	
RTS_n/TDO/GPIO9	IO	Note3	Note4	0	0	Y	Note5	
DTR_n/GPIO10	IO	Note3	Note4	0	0	Y	Note5	
CTS_n/TMS/GPIO11	IO	Note3	Note4	0	0	Y	Note5	
DSR_n/TCK/GPIO12	IO	Note3	Note4	0	0	Y	Note5	
DCD_n/TDI/GPIO13	IO	Note3	Note4	0	0	Y	Note5	
RI_n/GPIO14	IO	Note3	Note4	0	0	Y	Note5	
RTCAS/GPIO15	IO	Note3	Note4	0	0	Y	S	
RTCRD/GPIO16	IO	Note3	Note4	0	0	Y	S	
RTCWR/GPIO17	IO	Note3	Note4	0	0	Y	S	
IRQ8_n/GPIO18	IO	Note3	Note4	0	0	Y	S	
REXT	I							
OVRCUR_n	I	--	1	0	1	Y	--	
DP1, DM1	IO							
DP2, DM2	IO							
A20GATE_n/ GPIO54	IO	16mA	Note4	0	0	Y	F	
KBRST_n/ GPIO55	IO	16mA	Note4	0	0	Y	F	
SPEAKER/GPIO53	IO	Note3	Note4	0	0	Y	S	
CLK25MOUT/ GPIO56	IO	16mA	Note4	0	0	Y	F	
XCS1_n/GPIO57	IO	16mA	Note4	0	0	Y	F	
XCS2_n/GPIO58	IO	16mA	Note4	0	0	Y	F	

Note 1: *Programmable, default is 16mA.*
Note 2: *Programmable, default is Fast.*
Note 3: *Programmable, default is 4mA.*
Note 4: *Programmed by the GPIO mode & dir. Register.*
Note 5: *Programmable, default is slow.*
Note 6: *The pins never in the driving current, pull-up, pull-down, schimitt trigger, I/O pad, and slew rate status are not shown in the above table.*
Note 7: *A PCI type IO pad.*
Note 8: *This Pin is programmable.*
Note 9: *The Pulldown defaults to '0' but is programmable.*

5. System Address Map

The R3210 microprocessor supports 4 Gbytes of addressable memory space and 64 Kbytes of addressable I/O space. In order to be compatible with PC/AT system, the lower 1 Mbytes of this addressable memory is divided into regions which can be individually controlled with programmable attributes such as disable, read/write, write only, or read only (see Chapter 11, Register Description section for details on attribute programming).

5.1 Memory Address Ranges

Figure 5-1 represents R3210 mircoprocessor memory address map. It shows the main memory regions defined and supported by the R3210. At the highest level, the address space is divided into two main conceptual regions. One is the 0–1-Mbyte DOS compatibility region and the other is 1-Mbyte to 4-Gbyte extended memory region. The R3210 processor supports several main memory sizes from 2MB to 128MB. The main memroy type and size in the system will be auto-detected by the system BIOS.

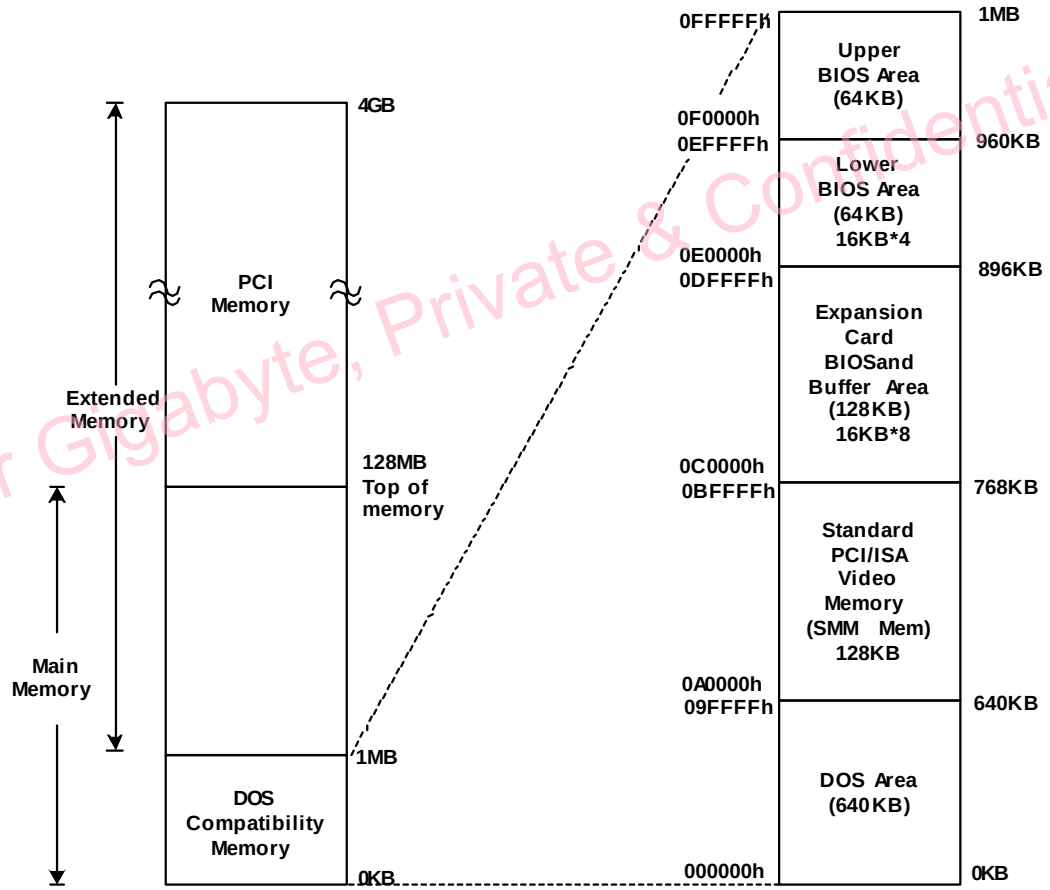


Figure 5-1. Memory Address Map

5.1.1 Dos Compatibility Region

The first region of memory is called the Dos Compatibility Region because it is defined for early PC. This area is divided into the following address regions:

- 0–640-Kbyte DOS Area
- 640–768-Kbyte Video Buffer Area
- 768–896-Kbyte in 16-Kbyte sections (total of 8 sections) - Expansion Area
- 896–960-Kbyte in 16-Kbyte sections (total of 4 sections) - Extended System BIOS Area
- 960-Kbyte–1-Mbyte Memory (BIOS Area) - System BIOS Area

From 640 Kbytes – 1Mbytes: it can be divided into fourteen ranges which can be enabled or disabled independently for both read and write. These regions can also be mapped to either main DRAM or PCI by system BIOS. (See A/B Page Control Register and Memory Attribute Register in Section 3, Chapter 11.)

DOS Area (00000–9FFFFh)

The DOS area (00000h – 9FFFFh) is 640 Kbytes in size. It is always mapped to the main memory controlled by the R3210 microprocessor.

Video Buffer Area (A0000–BFFFFh)

The 128-Kbyte graphics adapter memory region is normally mapped to a video device on the PCI bus (typically VGA controller). This area is controlled by the A/B Page Control Register. It can be mapped to either main DRAM or PCI for both read and write command.

ISA Expansion Area (C0000–DFFFFh)

This 128-Kbyte ISA Expansion region is divided into eight 16-Kbyte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the PCI bridge to ISA space. Memory that is disabled is not remapped.

Extended System BIOS Area (E0000–EFFFFh)

This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to PCI. Typically, this area is used for RAM or ROM. Memory that is disabled is not remapped.

System BIOS Area (F0000–FFFFFh)

This area is a single 64-Kbyte segment that can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to PCI. By manipulating the read/write attributes, the R3210 microprocessor can “shadow” BIOS into main memory. Memory that is disabled is not remapped.

5.1.2 Extended Memory Region

This memory region covers 10_0000h (1 Mbytes) to FFFF_FFFFh (4 Gbytes minus 1) address range and is divided into the following regions:

- DRAM memory from 1 Mbytes to a top of memory (maximum: 128 Mbytes)
- PCI Memory space from the top of memory to 4 Gbytes
- APIC Configuration Space from FEC00000h (4 Gbytes minus 20 Mbytes) to FEC0_FFFFh
- High BIOS area from 4 Gbytes to 4 Gbytes minus 2 Mbytes

Main DRAM Address Range (0010_0000h to Top of Main Memory)

The address range from 1 Mbytes to the top of main memory is mapped to the main memory address range controlled by the R3210 microprocessor. All accesses to addresses within this range are forwarded to the main memory.

PCI Memory Address Range (Top of Main Memory to 4 Gbytes)

The address range from the top of main DRAM to 4 Gbytes is normally mapped to PCI. The PMC forwards all accesses within this address range to PCI.

Within this address range, there are two sub-ranges defined as APIC Configuration Space and High BIOS Address Range.

1. High BIOS Area (FFE0_0000–FFFF_FFFFh)

The top 2 Mbytes of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to the PCI so that the upper subset of this region is aliased to 16 Mbytes minus 256 Kbytes range. The actual address space required for the BIOS is less than 2 Mbytes. However, the minimum CPU MTRR range for this region is 2 Mbytes. Thus, the full 2 Mbytes must be considered.

5.2 Memory Shadowing

Any block of memory that can be designated as read only or write only can be “shadowed” into PMC DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read only during the copy process while DRAM at the same time is designated write only. After copying, the DRAM is designated read only so that ROM is shadowed. CPU bus transactions are routed accordingly. The PMC does not respond to transactions originating from PCI or ISA masters and targeted at shadowed memory blocks.

5.3 I/O Address Space

The R3210 positively decodes accesses to all internal registers, including PCI configuration registers (CF8h and CFCh), PC/AT Compatible IO registers (8237, 8254 & 8259), and all relocatable IO space registers (UART).

6. Operation Mode

The R3210 microprocessor supports three operation modes: protected mode, real-address mode, and system management mode. The operation mode determines which instructions and architectural features are accessible:

• **Protected mode.** In this mode all instructions and architectural features are available, providing the highest performance and capability. This is the recommended mode for all new applications and operating systems.
Among the capabilities of protected mode is the ability to directly execute “real-address mode” 8086 software in a protected, multitasking environment. This feature is called virtual-8086 mode, although it is not actually a processor mode. Virtual-8086 mode is actually a protected mode attribute that can be enabled for any task.
• **Real-address mode.** It provides the programming environment of the Intel 8086 processor with a few extensions (such as the ability to switch to protected or system management mode). The processor is placed in real-address mode following power-up or a reset.

7. Register Sets

The R3210 contains three sets of software accessible registers (Core registers, I/O Mapped registers and Configuration registers).

7.1 Core Registers

The R3210 microprocessor provides 24 Core Registers. The 16 Base Architecture Registers (General-purpose Registers, Segment Registers, Flags Register and Instruction Pointer) are used in general system and application programming. The other 8 system-level registers (Control Registers and System Address Registers) can be used only by system-level programs. These registers are shown below. The details will be described in Register Description in Chapter 11.

7.1.1 General-Purpose Registers

Register Name	Context Location
EAX	11.1.1
EBX	11.1.1
ECX	11.1.1
EDX	11.1.1
ESI	11.1.1
EDI	11.1.1
EBP	11.1.1
ESP	11.1.1

7.1.2 Segment Registers

Register Name	Context Location
Code Segment Register – CS	11.1.2
Stack Segment Register – SS	11.1.2
Data Segment Register – DS	11.1.2
Data Segment Register – ES	11.1.2
Data Segment Register – FS	11.1.2
Data Segment Register – GS	11.1.2

7.1.3 Flags Register

Register Name	Context Location
Flags Register	11.1.4

7.1.4 Instruction Pointer

Register Name	Context Location
Instruction Pointer	11.1.3

7.1.5 Control Registers

Register Name	Context Location
Control Register 0	11.1.5
Control Register 1	11.1.5
Control Register 2	11.1.5
Control Register 3	11.1.5

7.1.6 System Address Registers

Register Name	Context Location
Global Descriptor Table Register	11.1.6
Interrupt Descriptor Table Register	11.1.6
Local Descriptor Table Register	11.1.6
Task State Segment Register	11.1.6

7.2 I/O Mapped Registers

The I/O Mapped Registers are usually used to control the R3210 integrated peripherals or to store the peripherals' data, addresses and statuses. We divided these I/O Mapped Registers into fourteen subsets, including **PCI Configurations Registers**, **Slave DMA Controller Registers**, **DMA Page Registers**, **Master DMA Controller Registers**, **DMA High Page Registers**, **Timer / Counter Registers**, **Interrupt Edge/Level Control Registers**, **NMI Status and Control Register**, **CMOS Memory & RTC Registers**, **System Control Register** and **Serial Port Registers**. These registers have fixed IO Address except Serial Port Registers.

The base address of Serial Port Registers is programmable via the Internal UART IO Address Register in R3210_SB Configuration Space Register.

These registers are listed as below. In Chapter 11, Register Description will show more detailed information about these registers.

7.2.1 PCI Configuration Registers

IO Address	Register Name	Context Location
0CFBh-0CF8h	PCI Configuration Address Register	11.2.1
0CFFh-0CFCh	PCI Configuration Data Register	11.2.1

7.2.2 Slave DMA Controller Registers

IO Address	Register Name	Context Location
00h	Slave DMA Channel 0 Base/Current Address	11.2.2
01h	Slave DMA Channel 0 Base/Current Count	11.2.2
02h	Slave DMA Channel 1 Base/Current Address	11.2.2
03h	Slave DMA Channel 1 Base/Current Count	11.2.2
04h	Slave DMA Channel 2 Base/Current Address	11.2.2
05h	Slave DMA Channel 2 Base/Current Count	11.2.2
06h	Slave DMA Channel 3 Base/Current Address	11.2.2
07h	Slave DMA Channel 3 Base/Current Count	11.2.2
08h	Slave DMA Read Status / Write Command	11.2.2
09h	Slave DMA Read Request / Write Request	11.2.2
0Ah	Slave DMA Read Command / Write Single Mask	11.2.2
0Bh	Slave DMA Read / Write Mode	11.2.2
0Ch	Slave DMA Set / Clear First / Last Clear F/F	11.2.2
0Dh	Slave DMA Read Temporary / Master Clear	11.2.2
0Eh	Slave DMA Clear Mode Register. Counter / Clear Mask	11.2.2
0Fh	Slave DMA Write Mask	11.2.2

7.2.3 DMA Page Registers

IO Address	Register Name	Context Location
81h	DMA Page – DMA Channel 2	11.2.3
82h	DMA Page – DMA Channel 3	11.2.3
83h	DMA Page – DMA Channel 1	11.2.3
87h	DMA Page – DMA Channel 0	11.2.3
89h	DMA Page – DMA Channel 6	11.2.3
8Ah	DMA Page – DMA Channel 7	11.2.3
8Bh	DMA Page – DMA Channel 5	11.2.3

7.2.4 Master DMA Controller Registers

IO Address	Register Name	Context Location
C0h	Master DMA Channel 4 Base/Current Address	11.2.4
C2h	Master DMA Channel 4 Base/Current Count	11.2.4
C4h	Master DMA Channel 5 Base/Current Address	11.2.4
C6h	Master DMA Channel 5 Base/Current Count	11.2.4
C8h	Master DMA Channel 6 Base/Current Address	11.2.4
CAh	Master DMA Channel 6 Base/Current Count	11.2.4
CCh	Master DMA Channel 7 Base/Current Address	11.2.4
CEh	Master DMA Channel 7 Base/Current Count	11.2.4
D0h	Master DMA Read Status / Write Command	11.2.4
D2h	Master DMA Command/Request Register	11.2.4
D4h	Master DMA Read Command / Write Single Mask	11.2.4
D6h	Master DMA Read / Write Mode	11.2.4
D8h	Master DMA Set / Clear First / Last Clear F/F	11.2.4
DAh	Master DMA Read Temporary / Master Clear	11.2.4
DCh	Master DMA Clear Mode Register. Counter / Clear Mask	11.2.4
DEh	Master DMA Read / Write Mask	11.2.4

7.2.5 DMA High Page Registers

IO Address	Register Name	Context Location
481h	DMA High Page – DMA Channel 2.	11.2.5
482h	DMA High Page – DMA Channel 3.	11.2.5
483h	DMA High Page – DMA Channel 1.	11.2.5
487h	DMA High Page – DMA Channel 0.	11.2.5
489h	DMA High Page – DMA Channel 6.	11.2.5
48Ah	DMA High Page – DMA Channel 7.	11.2.5
48Bh	DMA High Page – DMA Channel 5.	11.2.5

7.2.6 Timer/Counter Registers

IO Address	Register Name	Context Location
40h	Timer / Counter 0 Count	11.2.6
41h	Timer / Counter 1 Count	11.2.6
42h	Timer / Counter 2 Count	11.2.6
43h	Timer / Counter Control	11.2.6

7.2.7 Master Interrupt Controller Registers

IO Address	Register Name	Context Location
20h	Master Interrupt Control/Interrupt Service/Interrupt Command	11.2.7
21h	Master Interrupt Mask	11.2.7

7.2.8 Slave Interrupt Controller Registers

IO Address	Register Name	Context Location
A0h	Slave Interrupt Request/Interrupt Service/Interrupt Command	11.2.8
A1h	Slave Interrupt Mask	11.2.8

7.2.9 Interrupt Edge/Level Control Registers

IO Address	Register Name	Context Location
4D0h	Master Interrupt Edge/Level Control	11.2.9
4D1h	Slave Interrupt Edge/Level Control	11.2.9

7.2.10 NMI Status and Control Register

IO Address	Register Name	Context Location
61h	NMI Status and Control Register	11.2.11

7.2.11 CMOS Memory & RTC Registers

IO Address	Register Name	Context Location
70h	CMOS Memory Address Register	11.2.12
71h	CMOS Memory Data Register	11.2.12

7.2.12 System Control Register

IO Address	Register Name	Context Location
92h	System Control	11.2.13

7.2.13 Serial Port Registers

(**B**ase **A**ddress Refers to the Register of index 57h-54h, IDSEL = AD18/SB of PCI Configuration Register)

IO Address	Register Name	Context Location
BA + 0h	Transmit/Receive Data Buffer (DLAB=0)	11.2.10
BA + 0h	LSB of Baud Rate Generator Divisor Latches (DLAB=1)	11.2.10
BA + 1h	Interrupt Enable Register (DLAB=0)	11.2.10
BA + 1h	MSB of Baud Rate Generator Divisor Latches (DLAB=1)	11.2.10
BA + 2h	Interrupt Identification Register	11.2.10
BA + 2h	FIFO Control Register	11.2.10
BA + 3h	Line Control Register	11.2.10
BA + 4h	Modem Control Register	11.2.10
BA + 5h	Line Status Register	11.2.10
BA + 6h	Modem Status Register	11.2.10
BA + 7h	Scratchpad Register	11.2.10

7.2.14 Fast Ethernet MAC Registers

(**B**ase **A**ddress Refers to the Register of index 10h/14h, IDSEL = AD19/AD20 of PCI Configuration Register)

IO Address	Register Name	Mnemonic	Context Location
BA + 00h	MAC Control Register 0	**MCR0**	13.3
BA + 04h	MAC Control Register 1	**MCR1**	13.4
BA + 08h	MAC Bus Control Register	**MBCR**	13.5
BA + 0Ch	MAC TX Interrupt Control Register	**MTICR**	13.6
BA + 10h	MAC RX Interrupt Control Register	**MRICR**	13.7
BA + 14h	MAC TX Poll Command Register	**MTPR**	13.8
BA + 18h	MAC RX Buffer Size Register	**MRBSR**	13.9
BA + 1Ah	MAC RX Descriptor Control Register	**MRDCR**	13.10
BA + 1Ch	MAC Last Status Register	**MLSR**	13.11
BA + 20h	MAC MDIO Control Register	**MMDIO**	13.12
BA + 24h	MAC MDIO Read Data Register	**MMRD**	13.13
BA + 28h	MAC MDIO Write Data Register	**MMWD**	13.14
BA + 2Ch	MAC TX Descriptor Start Address 0 Register	**MTDSA0**	13.15
BA + 30h	MAC TX Descriptor Start Address 1 Register	**MTDSA1**	13.16
BA + 34h	MAC RX Descriptor Start Address 0 Register	**MRDSA0**	13.17
BA + 38h	MAC RX Descriptor Start Address 1 Register	**MRDSA1**	13.18
BA + 3Ch	MAC INT Status Register	**MISR**	13.19
BA + 40h	MAC INT Enable Register	**MIER**	13.20
BA + 44h	MAC Event Counter INT Status Register	**MECISR**	13.21
BA + 48h	MAC Event Counter INT Enable Register	**MECIER**	13.22
BA + 50h	MAC Successfully Received Packet Counter Register	**MRCNT**	13.23
BA + 52h	MAC Event Counter 0 Register	**MECNT0**	13.24
BA + 54h	MAC Event Counter 1 Register	**MECNT1**	13.25
BA + 56h	MAC Event Counter 2 Register	**MECNT2**	13.26
BA + 58h	MAC Event Counter 3 Register	**MECNT3**	13.27
BA + 5Ah	MAC Successfully Transmit Packet Counter Register	**MTCNT**	13.28
BA + 5Ch	MAC Event Counter 4 Register	**MECNT4**	13.29
BA + 5Eh	MAC Pause Frame Counter Register	**MPCNT**	13.30
BA + 60h	MAC Hash Table Word 0	**MAR0**	13.31
BA + 62h	MAC Hash Table Word 1	**MAR1**	13.31
BA + 64h	MAC Hash Table Word 2	**MAR2**	13.31
BA + 66h	MAC Hash Table Word 3	**MAR3**	13.31
BA + 68h	MAC Multicast Address first two bytes Register	**MID0L**	13.32
BA + 6Ah	MAC Multicast Address second two bytes Register	**MID0M**	13.32
BA + 6Ch	MAC Multicast Address last two bytes Register	**MID0H**	13.32
BA + 70h	MAC Multicast Address first two bytes Register	**MID1L**	13.33
BA + 72h	MAC Multicast Address second two bytes Register	**MID1M**	13.33
BA + 74h	MAC Multicast Address last two bytes Register	**MID1H**	13.33
BA + 78h	MAC Multicast Address first two bytes Register	**MID2L**	13.34
BA + 7Ah	MAC Multicast Address second two bytes Register	**MID2M**	13.34
BA + 7Ch	MAC Multicast Address last two bytes Register	**MID2H**	13.34
BA + 80h	MAC Multicast Address first two bytes Register	**MID3L**	13.35
BA + 82h	MAC Multicast Address second two bytes Register	**MID3M**	13.35
BA + 84h	MAC Multicast Address last two bytes Register	**MID3H**	13.35
BA + 88h	MAC PHY Status Change Configuration Register	**MPSCCR**	13.36
BA + 8Ah	MAC PHY Status Register	**MPSR**	13.37
BA + BEh	MAC Identifier Register	**MACID**	13.38

7.2.15 USB 1.1 OHCI Operation Registers

(**B**ase **A**ddress Refers to the Register of index 10hh, IDSEL = AD21, Function 0 of PCI Configuration Register)

IO Address	Register Name	Context Location
BA + 00h	HC Revision Register	12.5.2.2
BA + 04h	HC Control Register	12.5.2.2
BA + 08h	HC Command Status Regster	12.5.2.2
BA + 0Ch	HC Interrupt Status Regster	12.5.2.2
BA + 10h	HC Interrupt Enable Regster	12.5.2.2
BA + 14h	HC Interrupt Disable Register	12.5.2.2
BA + 18h	HC HCCA Register	12.5.2.3
BA + 1Ch	HC Period Current ED Regster	12.5.2.3
BA + 20h	HC Control Head ED Regster	12.5.2.3
BA + 24h	HC Control Current ED Register	12.5.2.3
BA + 28h	HC Bulk Head ED Register	12.5.2.3
BA + 2Ch	HC Bulk Current ED Register	12.5.2.3
BA + 30h	HC Done Head Register	12.5.2.3
BA + 34h	HC Fm Interval Register	12.5.2.4
BA + 38h	HC Fm Remaining Register	12.5.2.4
BA + 3Ch	HC Fm Number Register	12.5.2.4
BA + 40h	HC Periodic Start Register	12.5.2.4
BA + 44h	HC LS Threshold Register	12.5.2.4
BA + 48h	HC Rh Descriptor A Register	12.5.2.5
BA + 4Ch	HC Rh Descriptor B Register	12.5.2.5
BA + 50h	HC Rh Status Register	12.5.2.5
BA + 54h	HC Rh Port Status [1] Register	12.5.2.5
BA + 58h	HC Rh PortStatus [2] Register	12.5.2.5
BA + 100h	HC eControl Register	12.5.2.6
BA + 104h	HC eInput Register	12.5.2.6
BA + 108h	HC eOutput Register	12.5.2.6
BA + 10Ch	HC eStatus Register	12.5.2.6

7.2.16 USB 2.0 EHCI Operation Registers

(**B**ase **A**ddress Refers to the Register of index 10h, IDSEL = AD21, Function 1 of PCI Configuration Register)

IO Address	Register Name	Mnemonic	Context Location
BA + 00h	Capability Register Length Register	**CAPLENGTH**	12.5.4.1
BA + 03h – 02h	USB1.1 Port Override Register	**HCIVERSION**	12.5.4.1
BA + 07h – 04h	Structural Parameters Register	**HCSPARAMS**	12.5.4.1
BA + 0Bh – 08h	Capability Parameters Register	**HCCPARAMS**	12.5.4.1
BA + 23h – 20h	USB2.0 Command Register	**USB2CMD**	12.5.4.2
BA + 27h – 24h	USB2.0 Status Register	**USB2STS**	12.5.4.2
BA + 2Bh – 28h	USB2.0 Interrupt Enable Register	**USB2INTR**	12.5.4.2
BA + 2Fh – 2Ch	USB2.0 Frame Index register	**FRINDEX**	12.5.4.2
BA + 37h – 34h	Periodic Frame List Base Address Register	**PERIODICLISTBASE**	12.5.4.2
BA + 3Bh – 38h	Current Asynchronous List Address Register	**ASYNCLISTADDR**	12.5.4.2
BA + 63h – 60h	Configured Flag Register	**CONFIGFLAG**	12.5.4.2
BA + 6Bh – 64h	Port Status/Control Register	**PORTSC(0-1)**	12.5.4.2

7.3 Configuration Space Registers

The R3210 microprocessor integrated two PCI base bridges – Host-to-PCI bridge, ISA-to-PCI bridge, two MACs, one USB1.1 host and one USB2.0 host. These two bridges contain their own PCI Configuration Space. Configuration Space Registers reside in PCI Configuration Space and specify PCI configuration, DRAM configuration, operating parameters, and optional system features.

During hardware reset, the R3210 sets its internal configuration registers to predetermine default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the registers accordingly.

7.3.1 R3210_NB Configuration Space Registers (IDSEL = AD11/Device 0)

Offset (HEX)	Register Name	Context Location
01h – 00h	Vendor ID Register	11.3.1
03h – 02h	Device ID Register	11.3.1
05h – 04h	Command Register	11.3.1
07h – 06h	Status Register	11.3.1
08h	Revision ID Register	11.3.1
0Bh – 09h	Class Code Register	11.3.1
0Ch	Cache Line Size Register	11.3.1
0Eh	Header Type Register	11.3.1
2Dh – 2Ch	Subsystem Vendor ID Register	11.3.1
2Fh – 2Eh	Subsystem Device ID Register	11.3.1
53h – 50h	Non-Cache Region Register #1 for L1	11.3.1
57h – 40h	Non-Cache Region Register #2 for L1	11.3.1
5Bh – 58h	Non-Cache Region Register #3 for L1	11.3.1
5Fh – 5Ch	Non-Cache Region Register #4 for L1	11.3.1
66h	Memory Clock Phase Selection Register	11.3.1
69h – 68h	Memory Timing Register	11.3.1
6Bh – 6Ah	Memory Control Register	11.3.1
6Dh – 6Ch	Memory Bank Register	11.3.1
6E	Memory Read/Write Reorder & Refresh Register	11.3.1
83h	A/B Page Control Register	11.3.1
87h – 84h	Memory Attribute Register	11.3.1
93h – 90h	Customer ID Register	11.3.1
97h – 94h	Spare 1 Register	11.3.1
9Bh – 98h	Spare 2 Register	11.3.1
9Fh – 9Ch	Spare 3 Register	11.3.1
C3h – C0h	USB PHY Control and BIST Control Register	11.3.1

7.3.2 R3210_SB Configuration Space Registers (IDSEL = AD18/Device 7)

Offset (HEX)	Register Name	Context Location
01h – 00h	Vendor ID Register	11.3.2
03h – 02h	Device ID Register	11.3.2
05h – 04h	Command Register	11.3.2
07h – 06h	Status Register	11.3.2
08h	Revision ID Register	11.3.2
0Bh – 09h	Class Code Register	11.3.2
0Eh	Header Type Register	11.3.2
2Dh – 2Ch	Subsystem Vendor ID Register	11.3.2
2Fh – 2Eh	Subsystem Device ID Register	11.3.2
40h	Boot Strapping Register	11.3.2
41h	Write Lock and LPC Control Register	11.3.2
43h – 42h	Flash ROM Chip Select Control Register	11.3.2
46h – 44h	Watchdog Timer Control	11.3.2
4Bh – 48h	General-Purpose I/O Control Register I	11.3.2
4Fh – 4Ch	General-Purpose I/O Data Register I	11.3.2
50h	Serial IRQ (IRQSER) Control Register	11.3.2
51h	LPC Control Register	11.3.2
52h	LPC Legacy COM Port Decoding Register	11.3.2
53h	Internal UART Control Register	11.3.2
57h – 54h	Internal UART IO Address Register	11.3.2
5Bh – 58h	PCI Interrupt Routing Table Register	11.3.2
5Fh – 5Ch	Buffer Strength Control Register I	11.3.2
63h – 60h	Buffer Strength Control Register II	11.3.2

67h – 64h	Buffer Strength Control Register III	11.3.2
6Bh – 68h	Buffer Strength Control Register IV	11.3.2
80h	Internal Peripherals Test Mode Register	11.3.2
87h – 84h	General-Purpose I/O Control Register II	11.3.2
8Bh – 88h	General-Purpose I/O Data Register II	11.3.2
93h – 90h	Chip Select 1 Base Address Register	11.3.2
97h – 94h	Chip Select 1 Base Address Mask Register	11.3.2
9Bh – 98h	Chip Select 2 Base Address Register	11.3.2
9Fh – 9Ch	Chip Select 2 Base Address Mask Register	11.3.2

7.3.3 R3210_MAC1/2 Configuration Space Registers (IDSEL = AD19/Device 8/MAC1, AD20/Device 9/MAC2)

Offset (HEX)	Register Name	Context Location
01h – 00h	Vendor ID Register	11.3.3
03h – 02h	Device ID Register	11.3.3
05h – 04h	Command Register	11.3.3
07h – 06h	Status Register	11.3.3
08h	Revision ID Register	11.3.3
0Bh – 09h	Class Code Register	11.3.3
13h – 10h	I/O Base Address Register	11.3.3
17h – 14h	Memory Base Address Register	11.3.3
2Dh – 2Ch	Subsystem Vendor ID Register	11.3.3
2Fh – 2Eh	Subsystem Device ID Register	11.3.3
3Dh – 3Ch	Interrupt Control Register	11.3.3

7.3.4 R3210_USB1.1 Configuration Space Registers (IDSEL = AD21/Device 10/Function 0)

Offset (HEX)	Register Name	Context Location
01h – 00h	Vendor ID Register	12.5.1
03h – 02h	Device ID Register	12.5.1
05h – 04h	Command Register	12.5.1
07h – 06h	Status Register	12.5.1
08h	Revision ID Register	12.5.1
0Bh – 09h	Class Code Register	12.5.1
0Ch	Cache Line Size Register	12.5.1
0Dh	Latency Timer Register	12.5.1
0Eh	Header Type Register	12.5.1
13h – 10h	Base Address Register	12.5.1
2Dh – 2Ch	Subsystem Vendor ID Register	12.5.1
2Fh – 2Eh	Subsystem Device ID Register	12.5.1
3Dh – 3Ch	Interrupt Control Register	12.5.1
3Eh	Minimum Grant Register	12.5.1
3Fh	Max. Latency Register	12.5.1
44h	Operational Mode Enable Register I	12.5.1
45h	Operational Mode Enable Register II	12.5.1

46h	Operational Mode Enable Register III	12.5.1
49h – 48h	Operational Mode Enable Register IV	12.5.1

7.3.5 R3210_USB2.0 Configuration Space Registers (IDSEL = AD21/Device 10/Function 1)

Offset (HEX)	Register Name	Context Location
01h – 00h	Vendor ID Register	12.5.3.1
03h – 02h	Device ID Register	12.5.3.1
05h – 04h	Command Register	12.5.3.1
07h – 06h	Status Register	12.5.3.1
08h	Revision ID Register	12.5.3.1
0Bh – 09h	Class Code Register	12.5.3.1
0Ch	Cache Line Size Register	12.5.3.1
0Dh	Latency Timer Register	12.5.3.1
0Eh	Header Type Register	12.5.3.1

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8. Instruction Set

The R3210 RISC processor core instruction set can be divided into 11 categories of operations:

- Data Transfer
- Arithmetic
- Shift/Rotate
- String Manipulation
- Bit Manipulation
- Control Transfer
- High Level Language Support
- Operating System Support
- Processor Control

All the R3210 RISC processor core instructions operate on 0, 1, 2 or 3 operands, where an operand resides in a register, in the instruction itself or in memory. Most zero operand instructions (e.g., CLI, STI) take only one byte. One operand instruction is generally two bytes long. The average instruction is 3.2 bytes long. Since the R3210 RISC has a 32-byte instruction queue, an average of 10 instructions will be prefetched. The use of two operands permits the following types of common instructions:

- Register to Register
- Memory to Register
- Memory to Memory
- Immediate to Register
- Register to Memory
- Immediate to Memory

The operands can be 8-, 16-, or 32-bit long. As a general rule, when 32-bit code is being executed, operands are 8 or 32 bits; when the existing 80286 or 8086 code (16-bit code) is being executed, operands are 8 or 16 bits. Prefixes can be added to all instructions, which override the default length of the operands (i.e., use 32-bit operands for 16-bit code, or 16-bit operands for 32-bit code).

9. Addressing Modes

The R3210 RISC processor core provides a total of 11 addressing modes for instructions to specify operands. The addressing modes are optimized to allow the efficient execution of high-level languages such as C and FORTRAN, and they cover the vast majority of data references needed by high-level languages.

9.1 Register and Immediate Modes

Two of the addressing modes provide for instructions that operate on register or immediate operands:

Register Operand Mode: The operand is located in one of the 8-, 16- or 32-bit general registers.

Immediate Operand Mode: The operand is included in the instruction as part of the opcode.

9.2 32-Bit Memory Addressing Modes

The remaining 9 modes provide a mechanism for specifying the effective address of an operand. The linear address consists of two components: the segment base address and an effective address. The effective address is calculated by using combinations of the following four address elements:

Displacement: An 8-, or 32-bit immediate value, following the instruction.

Base: The contents of any general-purpose register. The base registers are generally used by compilers to point to the start of the local variable area.

Index: The contents of any general-purpose register except for ESP. The index registers are used to access the elements of an array, or a string of characters.

Scale: The index register's value can be multiplied by a scale factor: 1, 2, 4 or 8. Scaled index mode is especially useful for accessing arrays or structures.

Combinations of these 4 components make up the 9 additional addressing modes. There is no performance penalty for using any of these addressing combinations, since the effective address calculation is pipelined with the execution of other instructions. The one exception is the simultaneous use of Base and Index components, which require one additional clock.

The effective address (EA) of an operand is calculated according to the following formula.

EA = Base Reg + (Index Reg • Scaling) + Displacement

Direct Mode: The operand's offset is contained as part of the instruction as an 8-, 16- or 32-bit displacement.

Example: INC Word PTR [500]

Register Indirect Mode: A **Base** register contains the address of the operand.

Example: MOV [ECX], EDX

Based Mode: A **Base** register's contents are added to a **Displacement** to form the operand's offset.

Example: MOV ECX, [EAX + 24]

Index Mode: An **Index** register's contents are added to a **Displacement** to form the operand's offset.

Example: ADD EAX, TABLE[ESI]

Scaled Index Mode: An **Index** register's contents are multiplied by a **Scaling** factor that is added to a **Displacement** to form the operand's offset.

Example: IMUL EBX, TABLE[ESI • 4], 7

Based Index Mode: The contents of a **Base** register are added to the contents of an **Index** register to form the effective address of an operand.

Example: MOV EAX, [ESI] [EBX]

Based Scaled Index Mode: The contents of an **Index** register is multiplied by a **Scaling** factor and the result is added to the contents of a **Base** register to obtain the operand's offset.

Example: MOV ECX, [EDX • 8] [EAX]

Based Index Mode with Displacement: The contents of an **Index** register and a **Base** register's contents and a **Displacement** are all summed together to form the operand offset.

Example: ADD EDX, [ESI] [EBP + 00FFFFF0H]

Based Scaled Index Mode with Displacement: The contents of an **Index** register are multiplied by a **Scaling** factor and the result is added to the contents of a **Base** register and a **Displacement** to form the operand's offset.

Example: MOV EAX, LOCALTABLE [EDI • 4] [EBP + 80]

9.3 Differences between 16- and 32-bit Addresses

In order to provide software compatibility with the 80286 and 8086, the R3210 RISC processor core can execute 16-bit instructions in Real and Protected Modes. The processor determines the size of the instructions it is executing by examining the D bit in the CS segment Descriptor. If the D bit is 0, all operand lengths and effective addresses are assumed to be 16 bits long. If the D bit is 1, the default length for operands and addresses is 32 bits. In Real Mode, the default size for operands and addresses is 16 bits.

Regardless of the default precision of the operands or addresses, the R3210 RISC processor core is able to execute either 16- or 32-bit instructions. This is specified via the use of override prefixes. Two prefixes, the **Operand Size Prefix** and the **Address Length Prefix**, override the value of the D bit on an individual instruction basis.

Example: The R3210 RISC processor core is executing in Real Mode and the programmer needs to access the EAX registers. The assembler code for this might be MOV EAX, 32-bit MEMORYOP, and ASM486 Macro Assembler automatically determines that an Operand Size Prefix is needed and generates it.

Example: The D bit is 0, and the programmer wishes to use Scaled Index addressing mode to access an array. The Address Length Prefix allows the use of MOV DX, TABLE [ESI • 2]. The assembler uses an Address Length Prefix since, with D= 0, the default addressing mode is 16 bits.

Example: The D bit is 1, and the program wants to store a 16-bit quantity. The Operand Length Prefix is used to specify only a 16-bit value: MOV MEM16, DX.

The OPERAND LENGTH and Address Length Prefixes can be applied separately or in combination to any instruction. The address Length Prefix does not allow addresses over 64 Kbytes to be accessed in Real Mode. A memory address that exceeds FFFFH will result in a General Protection Fault. An Address Length Prefix only allows the use of the additional R3210 RISC addressing modes.

When executing 32-bit code, the R3210 RISC processor core uses either 8- or 32-bit displacements, and any register can be used as base or index registers. When executing 16-bit code, the displacements are either 8 or 16 bits, and the base and index register conform to the 80286 mode 1

10. Functional Description

The core of the R3210 32-bit microprocessor is an x86-like, 6-stage pipeline RISC CPU core. In addition, the R3210 includes a 16/32-bit SDRAM controller, PCI bus controller, AT/PC compatible peripheral (DMA controller, Interrupt controller and Timer), LPC Controller, X-bus interface and UART. The R3210 is a highly integrated SOC that is suitable for embedded system. With the inherent high performance of RDC CPU core, the R3210 enables the designers to take the advantage to implement a wide variety of performance intensive applications, such as IP sharing, access point, home gateway, and internet appliance, while still maintains the lowest overall system cost.

The following sections will discuss the sub-function of the R3210.

10.1 RDC RISC Processor

The R3210 integrates a high speed and high performance CPU core that is designed on RDC advanced 32-bit, 6-stage pipeline architecture and executes up to 66 MHz. The CPU core of R3210 implements an MMU (Memory Management Unit) with 32 TLB buffers. With the MMU, the R3210 is compatible with a wide variety of operating systems, including MS Windows, Linux and most popular modern RTOS.

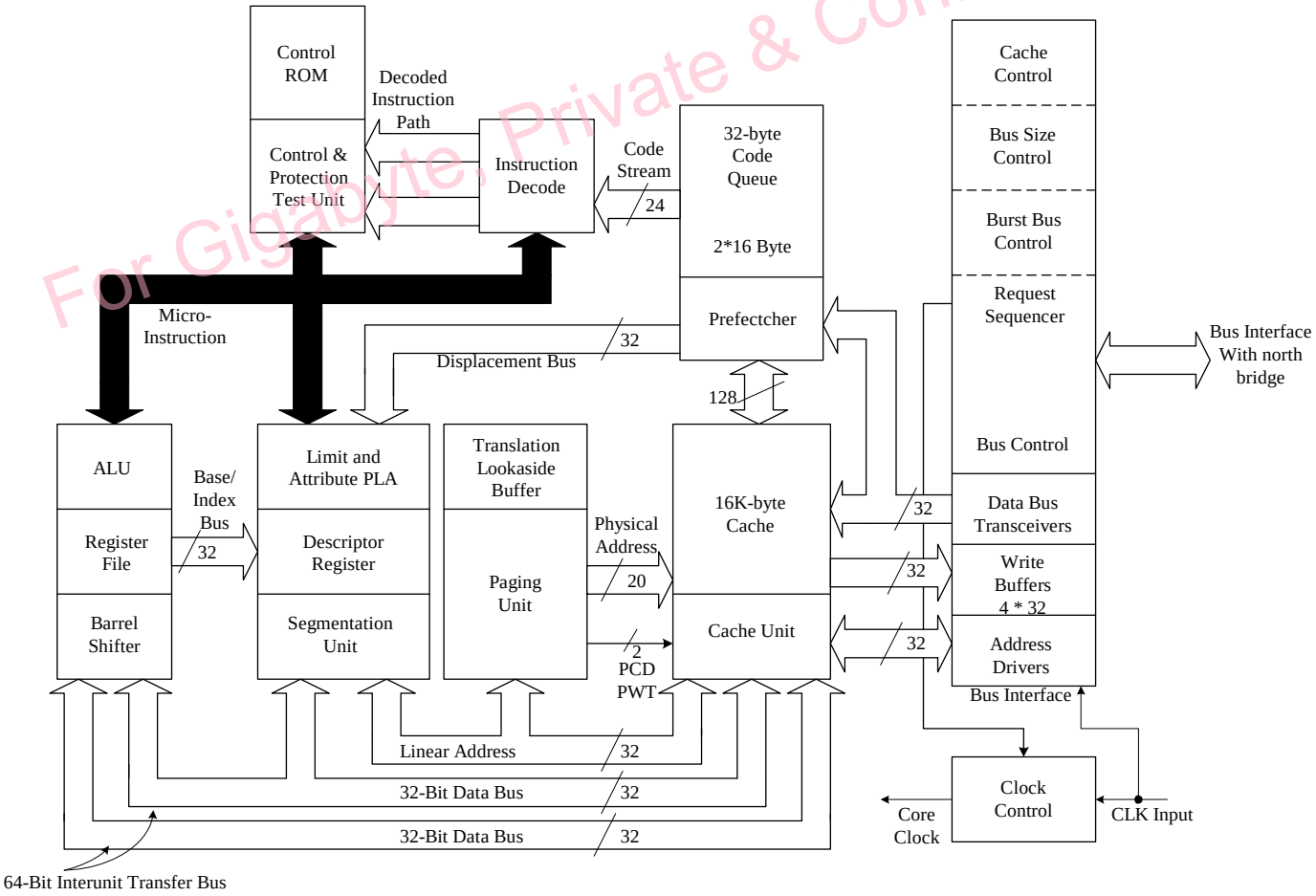


Figure 10-1. R3210 Core Processor Block Diagram

This R3210 RISC processor core contains all the features of the 486SX microprocessor with enhancements to increase its performance. The instruction set includes the complete 486SX microprocessor instruction set along with extensions to serve new applications.

Bus Unit

The bus unit manages data transfers, instruction prefetches and control functions between the processor's internal units and the R3210 NB. Internally, the bus unit communicates with the cache and the instruction prefetch units through the 32-bit bus. Externally, the bus unit provides the processor with bus functions, including external bus cycles, memory read/write, instruction fetch, cache line fill, etc.,

Prefetch Unit

When the BUS UNIT is not performing bus cycles to execute an instruction, the instruction prefetch unit uses the BUS UNIT to prefetch instructions. By reading instructions before they are needed, the processor rarely needs to wait for an instruction prefetch cycle on the processor bus.

Instruction prefetch cycles read 16-byte blocks of instructions, starting at addresses numerically greater than the last-fetched instruction. The prefetch unit, which has a direct connection to the paging unit, generates the starting address. The 16-byte prefetched blocks are read into both the prefetch and cache units simultaneously. The prefetch queue in the prefetch unit stores 32 bytes of instructions. As each instruction is fetched from the queue, the code part is sent to the instruction decode unit and (depending on the instruction) the displacement part is sent to the segmentation unit, where it is used for address calculation. If loops are encountered in the program being executed, the prefetch unit gets copies of previously executed instructions from the cache.

Decode Unit

The instruction decode unit receives instructions from the instruction prefetch unit and translates them in a two-stage process into low-level control signals and microcode entry points, as shown in Figure 10-.1. Most instructions can be decoded at a rate of one per clock.

The decode unit simultaneously processes instruction prefix bytes, opcodes, modR/M bytes, and displacements. The outputs include hardwired microinstructions to the segmentation, and integer units. The instruction decode unit is flushed whenever the instruction prefetch unit is flushed.

Memory Management Unit

The on-chip memory management unit (MMU) is completely compatible with the X86 microprocessor.

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatability and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be disabled by system software. Each segment can be divided into one or more 4 Kbytes segments. To implement a virtual memory system, full restartability for all page and segment faults is supported.

Memory is organized into one or more variable length segments, each up to four gigabytes (2^{32} bytes) in size. A segment can have attributes associated with it, which include its location, size, type (i.e., stack, code or data), and protection characteristics. Each task can have a maximum of 16,381 segments, each up to four gigabytes in size. Thus each task has a maximum of 64 terabytes (trillion bytes) of virtual memory.

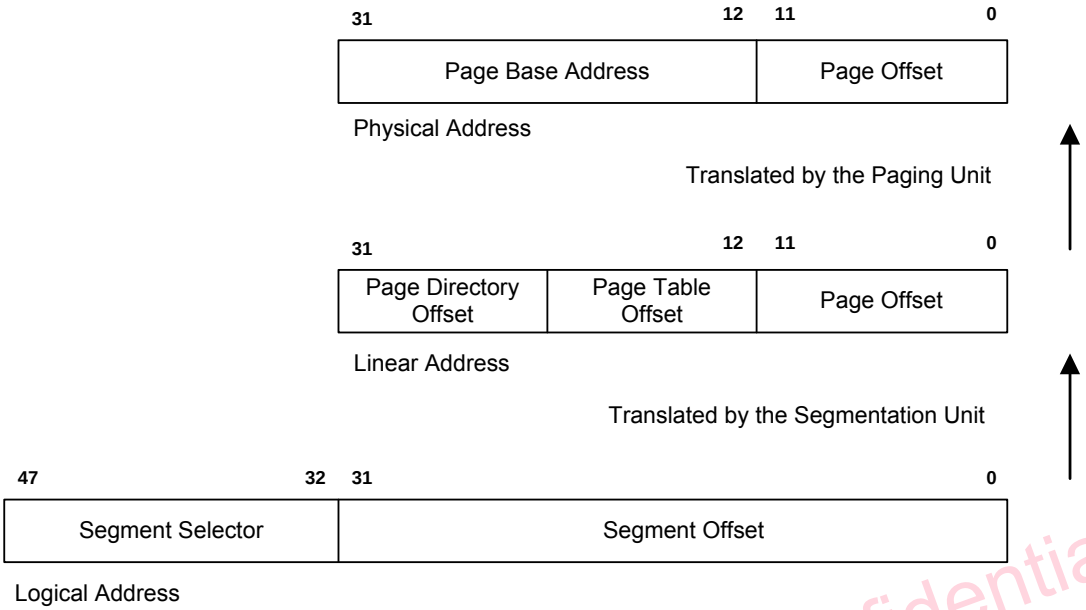


Figure 10-2. Segmentation and Paging Address Formats

The segmentation unit provides four levels of protection for isolating and protecting applications and the operating system from each other. The hardware-enforced protection allows the design of systems with a high degree of integrity.

10.2 L1 Cache

In order to maximize the performance, the R3210 integrated a direct map, 16Kbyte unified code and data cache in it. The level 1 cache supports write through policy. The on-chip L1 cache allows frequently used data and code to be stored on chip reducing accesses to the external bus. It significantly reduces the penalty of performance to access these codes and data from external slower memory devices.

10.3 SDRAM Controller

The R3210 integrates a main memory SDRAM controller that supports a 16-bit or 32-bit SDRAM data bus width. The R3210 SDRAM interface runs up to 133MHz. The thirteen multiplexed address lines, MA[12:0], and 2 SDRAM banks supported allow the R3210 to support maximum 128 Mbytes main memory space. All of SDRAM configurations provided by R3210 are listed as below:

- **16-bit data width:**

One Chip Select		
Memory Size	SDRAM Type	
	x 8	x 16
2MB		1Mb x 16 x 1
4MB	2Mb x 8 x 2	
8MB		4Mb x 16 x 1
16MB	8Mb x 8 x 2	8Mb x 16 x 1
32MB	16Mb x 8 x 2	16Mb x 16 x 1
64MB	32Mb x 8 x 2	

Two Chip Selects		
Memory Size	SDRAM Type	
	x 8	x 16
4MB		1Mb x 16 x 1
8MB	2Mb x 8 x 2	
16MB		4Mb x 16 x 1
32MB	8Mb x 8 x 2	8Mb x 16 x 1
64MB	16Mb x 8 x 2	16Mb x 16 x 1
128MB	32Mb x 8 x 2	

10.4 PCI Bus Controller

In order to leverage the wide availability of low-cost peripherals, as well as to simplify the design off add-in functions, the R3210 integrates a full 32-bit PCI bus interface. Key attributes of the PCI bus include:

- Supports PCI Rev 2.1 specification.
- 32-bit bus interface
- Supports PCI clock at 33 MHz.
- On-chip PCI arbiter
- Supports PCI master/slave
- Up to 133 Mbytes/sec maximum bandwidth
- Supports up to 3 external master devices on PCI
- Provides four PCI interrupt channels

PCI Bus Arbitration

The PCI Bus arbiter for the R3210 allows concurrent host and PCI transactions to main memory. The arbiter supports three external PCI masters in addition to the R3210. REQ_n[2:0]/GNT_n[2:0] are used by PCI masters.

10.5 DMA Controller

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Figure 10-3). Master DMA Controller (DMA-1) corresponds to DMA Channels 0–3 and Slave DMA Controller (DMA-2) corresponds to Channels 5–7. DMA Channel 4 is used to cascade the two controllers and will default to cascade mode in the DMA Channel Mode (DCM) Register. This channel is not available for any other purpose. In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that are initiated by software. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.

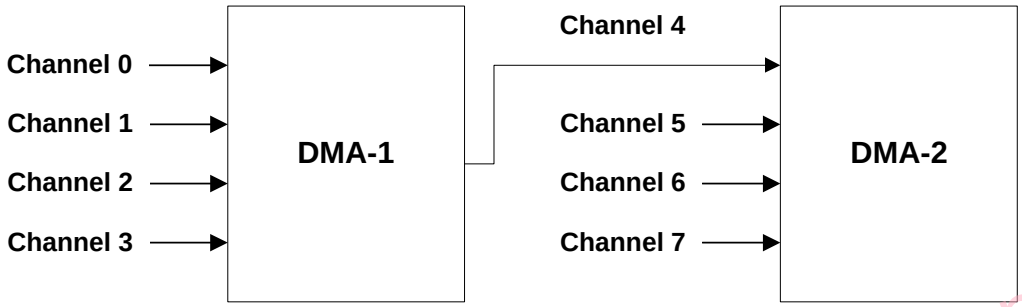


Figure 10-3. Internal DMA Controller

Each DMA channel is hardwired to the compatible settings for DMA device size: channel 3-0 are hardwired to 8-bit, count-by-bytes transfers, and channel 7-5 are hardwired to 16-bit, count-by-words (address shifted) transfers. The R3210 SB provides the timing control and data size translation necessary for the DMA transfer between the memory (ISA or DRAM) and the ISA Bus IO.

The R3210 SB provides 24-bit addressing in compliance with the ISA-Compatible specification. Each channel includes a 16-bit ISA-Compatible Current Register, which holds the 16 least-significant bits of the 24-bit address, an ISA-Compatible Page Register which contains the eight next most significant bits of address.

The DMA controller also features refresh address generation, and auto-initialization following a DMA termination.

The DMA controller is at any time either in master mode or slave mode. In master mode, the DMA controller is either servicing a DMA slave's request for DMA cycles, or allowing a 16-bit ISA master to use the bus via a cascaded DREQ signal. In slave mode, the R3210 SB monitors both the ISA Bus and PCI, decoding and responding to I/O read and write commands that address its registers.

Note that a DMA device (I/O device) is always on the ISA Bus, but the memory referenced is located on either an ISA Bus device or on PCI. When the R3210 SB is running a compatible DMA cycle, it drives the MEMR_n or MEMW_n strobes if the address is less than 16 Mbytes (000000h–FFFFFFh). These memory strobes are generated regardless of whether the cycle is decoded for PCI or ISA memory. The SMEMR_n and SMEMW_n are generated if the address is less than 1 Mbytes (0000000h–00FFFFFh). If the address is greater than 16 Mbytes (1000000h–7FFFFFFh), the MEMR_n or MEMW_n strobe is not generated to avoid aliasing issues.

10.5.1 DMA Transfer Modes

The channels can be programmed for any of four transfer modes. The transfer modes include single, block, demand, or cascade. Each of the three active transfer modes (single, block, and demand) can perform three different types of transfers (read, write or verify). Please note that R3210 SB does not support memory-to-memory transfers.

Single Transfer Mode

In single transfer mode, the DMA is programmed to make one transfer only. The byte/word count is decremented and the address decremented or incremented following each transfer. When the byte/word count "rolls over" from zero to FFFFh, a Terminal Count (TC) causes an auto-initialization if the channel has been programmed to do so.

To be recognized, DREQ must be held active until DACK_n becomes active. If DREQ is held active throughout the single transfer, the bus is released after a single transfer. With DREQ asserted high, the DMA I/O device rearbitrates for the bus. Upon winning the bus, another single transfer is performed. This allows other ISA bus masters a chance to acquire the bus.

Block Transfer Mode

In Block Transfer mode, the DMA is activated by DREQ to continue making transfers during the service until a TC, caused by either a byte/word count going to FFFFh, is encountered. DREQ need only be held active until DACK_n becomes active. If the channel has been programmed for it, an auto-initialization occurs at the end of the service. In this mode, it is possible to lock out other devices for a period of time (including refresh) if the transfer count is programmed to a large number.

Demand Transfer Mode

In Demand Transfer mode, the DMA channel is programmed to continue making transfers until a TC (Terminal Count) is encountered, or until the DMA I/O device releases DREQ. Thus, transfers may continue until the I/O device has exhausted its data capacity. After the I/O device catches up, the DMA service is re-established when the DMA I/O device reasserts the channel's DREQ. During the time between services when the system is allowed to operate, the intermediate values of address and byte/word count are stored in the DMA controller Current Address and Current Byte/Word Count Registers. A TC can cause an auto-initialize at the end of the service, if the channel has been programmed for it.

Cascade Mode

In Cascade Mode, the DMA controller will respond to DREQ with DACK, but R3210 SB will not drive IOR_n, IOW_n, MEMR_n, MEMW_n, LA[23:17], SA[19:0], and SBHE_n.

Cascade mode is also used to allow direct access of the system by 16-bit bus masters. These devices use the DREQ and DACK signals to arbitrate for the ISA Bus. The ISA master asserts its ISA master request line (DREQ[x]) to the DMA internal arbiter. If the ISA master wins the arbitration, R3210 SB responds with an ISA master acknowledge (DACK[x]) signal active. Upon sampling the DACK[x] line active, the ISA master takes control of the ISA Bus. While an ISA Master owns the bus, BALE is always driven high while AEN is always driven low. The ISA master has control of the ISA Bus and may run cycles until it negates the DREQ[x] line.

10.5.2 DMA Transfer Types

Each of the three active transfer modes (Single, Block, or Demand) can perform three different types of transfers. They are Read, Write and Verify.

Write Transfers

Write transfers move data from an ISA I/O device to memory located on the ISA Bus or in system DRAM. For transfers using compatible timing, R3210 SB will activate ISA Memory control signals to indicate a memory write as soon as the DMA provides the address. The PCI transfer is initiated after the data is valid on the ISA Bus. Data steering is used to steer the data to the correct byte lane during these DMA transfers. When the memory is located on the ISA Bus, a PCI cycle is not initiated.

The DMA device (I/O device) is either an 8- or 16-bit device and is located on the ISA Bus. The size of the DMA device is fixed for each channel.

Read Transfers

Read transfers move data from ISA memory or the system DRAM, to an ISA I/O device. R3210 SB activates the IOW_n command and the appropriate DRAM and ISA Memory control signals to indicate a memory read. Data steering is used to steer the data to the correct byte lane during these DMA transfers. When the cycle involves DRAM, the PCI read transaction is initiated as soon as the DMA address is valid. When the memory is located on the ISA Bus, a PCI cycle is not initiated.

Verify Transfer

Verify transfers are pseudo transfers. The DMA controller generates addresses as in normal read or write transfers. However, R3210 SB does not activate the ISA memory and I/O control lines. Only the DACK lines will go active. R3210 SB asserts the appropriate DACK signal for nine SYSCLKs. If Verify transfers are repeated during Block or Demand DMA requests, each additional pseudo transfer will add eight SYSCLKs. The DACK lines will not be toggled for repeated transfers.

10.5.3 DMA Timings

ISA-Compatible timing is provided for ISA DMA slave devices that reside on add in cards. The repetition rate for ISA-Compatible DMA cycles is eight SYSCLK periods.

When R3210 SB negates PHOLD_n one clock after driving FRAME_n asserted for a bus master IDE transaction, and another transaction is pending which will cause R3210 SB to acquire the PCI bus, it will drive PHOLD_n asserted for the next transaction three clocks after TRDY_n is driven negated for the current transaction.

10.5.4 DREQ and DACK_n Latency Control

The R3210 SB DMA arbiter maintains a minimum DREQ to DACK_n latency on all DMA channels when programmed in compatible mode. This is to support older devices such as the 8272A. The DREQs are delayed by eight SYSCLKs prior to being seen by the arbiter logic. This delay guarantees a minimum 1 msec DREQ to DACK_n latency. Software requests will not have this minimum request to DACK_n latency.

10.5.5 Channel Priority

For priority resolution, the DMA consists of two logical channel groups: channel 0–3 and channel 4–7. Each group may be in either fixed or rotate mode, as determined by the DMA Command Register.

DMA I/O slaves normally assert their DREQ line to arbitrate for DMA service. However, a software request for DMA service can be presented through each channel's DMA Request Register. A software request is subject to the same prioritization as any hardware request. Please see the detailed register description for Request Register programming information in the DMA Register description section.

Fixed Priority

The initial fixed priority structure is as follows:

High priority...Low priority
(0, 1, 2, 3) (5, 6, 7)

The fixed priority ordering is 0, 1, 2, 3, 5, 6, and 7. In this scheme, Channel 0 has the highest priority, and channel 7 has the lowest priority. Channel 3-0 of DMA-1 assume the priority position of Channel 4 in DMA-2, thus take the priority over channel 5, 6, and 7.

Rotating Priority

Rotation allows for "fairness" in priority resolution. The priority chain rotates so that the last channel serviced is assigned the lowest priority in the channel group (0–3, 5–7).

Channel 0–3 rotate as a group of four. They are always placed between Channel 5 and Channel 7 in the priority list.

Channel 5–7 rotate as part of a group of four. That is, channel 5–7 form the first three positions in the rotation, while channel group (0–3) comprises the fourth position in the arbitration.

10.5.6 Register Functionality

Please see the "DMA Register description" section for detailed information on register programming, bit definitions, and default values/functions of the DMA registers after CPURST is valid.

DMA Channel 4 is used to cascade the two DMA controllers together and should not be programmed for any mode other than cascade. The DMA Channel Mode Register for channel 4 will default to cascade mode. Special attention should also be taken when programming the Command and Mask Registers as related to channel 4.

10.5.7 Address Compatibility Mode

Whenever the DMA is operating, the addresses do not increment or decrement through the High and Low Page Registers. This is compatible with the 82C37 and Page Register implementation used in the PC-AT. This mode is set after CPURST is valid.

10.5.8 Summary of DMA Transfer Sizes

Table 10.1 lists each of the DMA device transfer sizes. The column labeled "Current Byte/Word Count Register" indicates that the register contents represent either the number of bytes to be transferred or the number of 16-bit words to be transferred. The column labeled "Current Address Increment/Decrement" indicates the number added to or taken from the Current Address register after each DMA transfer cycle. The DMA Channel Mode Register determines the Current Address Register will be incremented or decremented.

Table 10.1: DMA Transfer Size

DMA Device Date Size and Word Count	Current Byte/Word Count Register	Current Address Increment/Decrement
8-Bit I/O, Count by Bytes	Bytes	Bytes
16-Bit I/O, Count by Words (Address Shifted)	Words	1

10.5.8.1 Address Shifting When Programmed for 16-Bit I/O Count by Words

The R3210 SB maintains compatibility with the implementation of the DMA in the PC AT that uses the 82C37. The DMA shifts the addresses for transfers to/from a 16-bit device count-by-words. Note that the least significant bit of the Low Page Register is dropped in 16-bit shifted mode. When the Current Address Register is programmed (when the DMA channel is in this mode), the Current Address must be programmed to an even address with the address value shifted right by 1 bit. The address shifting is as follows:

Table 10.2: Address Shifting in 16-bit I/O DMA Transfers

Output Address	8-Bit I/O Programmed Address (Channel 0-3)	16-Bit I/O Programmed Address (Channel 5–7) (Shifted)
A0 A[16:1] A[23:17]	A0 A[16:1] A[23:17]	0 A[15:0] A[23:17]

Note:

The least significant bit of the Page Register is dropped in 16-bit shifted mode.

10.5.9 Autoinitialize

By programming a bit in the DMA Channel Mode Register, a channel may be set up as an autoinitialize channel. When a channel undergoes autoinitialization, the original values of the Current Page, Current Address and Current Byte/Word Count Registers are automatically restored from the Base Page, Address, and Byte/Word Count Registers of that channel following TC. The Base Registers are loaded simultaneously with the Current Registers by the microprocessor when the DMA channel is programmed and remains unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialize, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

10.5.10 Software Commands

There are three additional special software commands that can be executed by the DMA controller. The three software commands are:

1. Clear Byte Pointer Flip-Flop
2. Master Clear
3. Clear Mask Register

They do not depend on any specific bit pattern on the data bus.

Clear Byte Pointer Flip-Flop

This command is executed prior to writing or reading new address or word count information to/from the DMA controller. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

When the Host CPU is reading or writing DMA registers, two Byte Pointer flip-flops are used, one for channel 0–3 and one for channel 4–7. Both of these act independently. There are separate software commands for clearing each of them (0Ch for channel 0–3, 0D8h for channel 4–7).

DMA Master Clear

This software instruction has the same effect as the hardware reset. The Command, Status, Request, and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The DMA controller will enter the idle cycle.

There are two independent master clear commands; 0Dh which acts on channel 0–3, and 0DAh which acts on channel 4–7.

Clear Mask Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests. I/O port 00Eh is used for channel 0–3 and I/O port 0DCh for channel 4–7.

10.6 Programmable Timer

R3210 SB contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one timer unit, referred to as Timer-1. Each counter output provides a key system function. Counter 0 is connected to interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker. The 14.31818-MHz counters normally use OSC as a clock source.

Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation. The counter negates refresh request for one counter period (838 ns) during each count cycle. The initial count value is loaded one counter period after being written to the counter I/O address. The counter initially asserts refresh request, and negates it for one counter period when the count value reaches 1. The counter then asserts refresh request and continues counting from the initial count value.

Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h (see NMI Status and Control ports).

10.6.1 Programming the Interval Timer

The counter/timers are programmed by I/O accesses and are addressed as though they are contained in one 82C54 interval timer. A single Control Word Register controls the operation of all three counters. The interval timer is an I/O-mapped device. Several commands are available:

The Control Word Command specifies:

- which counter to read or write
- the operating mode
- the count format (binary or BCD)

The Counter Latch Command latches the current count so that it can be read by the system. The countdown process continues. The Read Back Command reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

The Read/Write Logic selects the Control Word Register during an I/O write when address lines A[1:0]=11. This condition occurs during an I/O write to port address 043h, the address for the Control Word Register on Timer 1. If the CPU writes to port 043h, the data is stored in the Control Word Register and is interpreted as the Control Word used to define the operation of the Counters.

The Control Word Register is write only. Counter status information is available with the read back Command.

Because the timer counters wake up in an unknown state after power up, multiple refresh requests may be queued. To avoid possible multiple refresh cycles after power up, program the timer counter immediately after power up.

Write Operations

Programming the interval timer is a simple process:

1. Write a control word.
2. Write an initial count for each counter.
3. Load the least and/or most significant bytes (as required by Control Word bit 5 and 4) of the 16-bit counter.

The programming procedure for the R3210 SB timer is very flexible. Only two conventions need to be observed. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three counters have separate addresses (selected by the A1 and A0 inputs), and each control word specifies the counter it applies to (SC0 and SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write 2-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

Interval Timer Control Word Format

The control word specifies the counter, the operating mode, the order and size of the count value, and whether it counts down in a 16-bit or binary-coded decimal (BCD) format. After writing the control word, a new count may be written at any time. The new value will take effect according to the programmed mode.

If a counter is programmed to read/write 2-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count. The count must always be completely loaded with both bytes.

Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress. There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read Back Command.

Counter I/O Port Read

The first method is to perform a simple read operation. To read the counter, which is selected with the A1 and A0 inputs (port 040h, 041h, or 042h), the CLK input of the selected counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result. When reading the count value directly, follow the format programmed in the control register: read LSB, read MSB, or read LSB then MSB. Within the R3210 SB timer unit, the GATE input on Counter 0 and Counter 1 is tied high. Therefore, the direct register read should not be used on these two counters. The GATE input of Counter 2 is controlled through I/O port 061h. If the GATE is disabled through this register, direct I/O reads of port 042h will return the current count value.

Counter Latch Command

The Counter Latch Command latches the count at the time the command is received. This command is used to ensure that the count read from the counter is accurate (particularly when reading a 2-byte count). The count value is then read from each counter's Count Register as was programmed by the Control Register.

The selected counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Each latched counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed mode of the counter in any way. The Counter Latch Command can be used for each counter in the R3210 SB timer unit.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read would be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the counter is programmed for 2-byte counts, 2 bytes must be read. The 2 bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

Another feature of the R3210 SB timer is that reads and writes of the same counter may be interleaved. For example, if the Counter is programmed for 2-byte counts, the following sequence is valid:

- Read least significant byte.
- Write new least significant byte.
- Read most significant byte.
- Write new most significant byte.

If a counter is programmed to read/write 2-byte counts, a program must not transfer control between reading the first and second byte to another routine which also reads from that same counter. Otherwise, an incorrect count will be read.

Read Back Command

The third method uses the Read Back Command. The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The Read Back Command is written to the Control Word Register, which causes the current states of the above-mentioned variables to be latched. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back Command may be used to latch multiple counter output latches (OL) by setting the COUNT_n bit D5=0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). Once read, a counter is automatically unlatched. The other counters remain latched until they are read. If multiple count Read Back Commands are issued to the same counter without reading the count, all but the first are ignored (i.e. the count which will be read is the count at the time the first Read Back Command was issued).

The Read Back Command may also be used to latch status information of selected counter(s) by setting STATUS_n bit D4=0. Status must be latched to be read. The status of a counter is accessed by a read from that counter's I/O port address.

If multiple counter status latch operations are performed without reading the status, all but the first are ignored. The status returned from the read is the counter status at the time the first status Read Back Command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both the COUNT_n and STATUS_n bits[5:4]=00. This is functionally the same as issuing two consecutive, separate Read Back Commands. The above discussions apply here also. Specifically, if multiple count and/or status Read Back Commands are issued to the same counter(s) without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter will return the latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return the latched count. Subsequent reads return unlatched count.

10.7 Programmable Interrupt Controller

R3210 SB provides an ISA-Compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers (Figure 10-4). The two controllers are cascaded, providing 13 external and three internal interrupts. The master interrupt controller provides IRQ[7:0] and the slave interrupt controller provides IRQ[15:8]. The three internal interrupts are used for internal functions only. IRQ0 is available to the user only when an external IO APIC is enabled. IRQ2 is used to cascade the two controllers and is not available to the user. IRQ0 is used as a system timer interrupt and is tied to Interval Timer 0, Counter 0. IRQ13 is reserved. The remaining 13 interrupt lines (IRQ[15:14,12:3,1]) are available for external system interrupts. IRQ[1] is fixed to edge trigger mode , IRQ[15:14, 12:3] edge or level sense selections are programmable on an individual channel-by-channel basis.

The Interrupt unit also supports interrupt steering. R3210 SB can be programmed to allow the four PCI active low interrupts (PIRQ[A:D]_n) to be internally routed to one of 11 interrupts (IRQ[15:14,12:9,7:3]).

The Interrupt Controller consists of two separate 82C59 cores. Interrupt Controller 1 (CNTRL-1) and Interrupt Controller 2 (CNTRL-2) are initialized separately and can be programmed to operate in different modes. The default settings are: 80x86 Mode, Edge Sensitive (IRQ[0:15]) Detection, Normal EOI, Non-Buffered Mode, Special Fully Nested Mode disabled, and Cascade Mode. CNTRL-1 is connected as the Master Interrupt Controller and CNTRL-2 is connected as the Slave Interrupt Controller.

Note that IRQ13 is generated internally (as part of the coprocessor error support) by R3210 SB. IRQ12/M is generated internally (as part of the mouse support) when bit-4 in the XBCS is set to a 1. When set to a 0, the standard IRQ12 function is provided and IRQ12 appears externally.

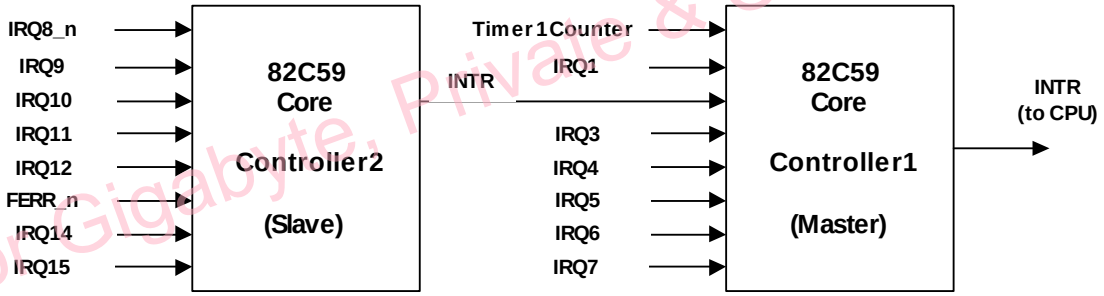


Figure 10-4. Interrupt Controller Block Diagram

10.7.1 Programming the Interrupt Controller

The Interrupt Controller accepts two types of command words generated by the CPU or bus master:

Initialization Command Words (ICWs)

Before normal operation begins, each Interrupt Controller in the system must be initialized. In the 82C59, this is a 2- to 4-byte sequence. However, for R3210 SB, each controller must be initialized with a 4-byte sequence. This 4-byte sequence is required to configure the interrupt controller correctly for the R3210 SB implementation. This implementation is ISA-Compatible.

The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4. The base address for each interrupt controller is a fixed location in the I/O memory space, at 0020h for CNTRL-1 and at 00A0h for CNTRL-2. An I/O write to the CNTRL-1 or CNTRL-2 base address with data bit 4 equal to 1 is interpreted as ICW1. For R3210 SB-based ISA systems, three I/O writes to "base address + 1" (021h for CNTRL-1 and 0A1h for CNTRL-2) must follow the ICW1. The first write to "base address + 1" (021h/0A1h) performs ICW2, the second write performs ICW3, and the third write performs ICW4.

ICW1 starts the initialization sequence. ICW2 is programmed to provide bits[7:3] of the interrupt vector that will be released onto the data bus by the interrupt controller during an interrupt acknowledge. A different base [7:3] is selected for each interrupt controller. ICW3 is programmed differently for CNTRL-1 and CNTRL-2, and has a different meaning for each controller.

For CNTRL-1, the master controller, ICW3 is used to indicate which IRQx input line is used to cascade CNTRL-2, the slave controller. Within the R3210 SB interrupt unit, IRQ2 on CNTRL-1 is used to cascade the INTR output of CNTRL-2. Consequently, bit 2 of ICW3 on CNTRL-1 is set to a 1, and the other bits are set to 0's.

For CNTRL-2, ICW3 is the slave identification code used during an interrupt acknowledge cycle. CNTRL-1 broadcasts a code to CNTRL-2 over three internal cascade lines if an IRQ[x] line from CNTRL-2 won the priority arbitration on the master controller and was granted an interrupt acknowledge by the CPU. CNTRL-2 compares this identification code to the value stored in ICW3, and if the code is equal to bits[2:0] of ICW3, CNTRL-2 assumes responsibility for broadcasting the interrupt vector during the second interrupt acknowledge cycle pulse.

ICW4 must be programmed on both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

Operation Command Words (OCWs)

These are the command words which dynamically reprogram the Interrupt Controller to operate in various interrupt modes. Any interrupt line can be masked by writing an OCW1. A 1 written in any bit of this command word will mask incoming interrupt requests on the corresponding IRQx line.

OCW2 is used to control the rotation of interrupt priorities when operating in the rotating priority mode and to control the End of Interrupt (EOI) function of the controller. OCW3 is used to set up reads of the ISR and IRR, to enable or disable the Special Mask Mode (SMM), and to set up the interrupt controller in polled interrupt mode. The OCWs can be written into the Interrupt Controller any time after initialization.

10.7.2 End-of-Interrupt Operation

End of Interrupt (EOI)

The In Service (IS) bit can be set to 0 automatically following the trailing edge of the second INTA_n pulse (when AEOI bit in ICW1 is set to 1) or by a command word that must be issued to the Interrupt Controller before returning from a service routine (EOI command). An EOI command must be issued twice with this cascaded interrupt controller configuration, once for the master and once for the slave.

There are two forms of EOI commands: Specific and Non-Specific. When the Interrupt Controller is operated in modes that preserve the fully nested structure, it can determine which IS bit to set to 0 on EOI. When a Non-Specific EOI command is issued, the Interrupt Controller automatically sets to 0 and the highest IS bit of those that are set to 1. Since in the fully nested mode, the highest IS level was necessarily the last level acknowledged and serviced. A Non-Specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used that may disturb the fully nested structure, the Interrupt Controller may no longer be able to determine the last level acknowledged. In this case, a Specific End of Interrupt must be issued that includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0–L2 is the binary level of the IS bit to be set to 0).

Note that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the Interrupt Controller is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

If AEOI=1 in ICW4, then the Interrupt Controller operates in AEOI mode continuously until reprogrammed by ICW4. Note that reprogramming ICW4 implies that ICW1, ICW2, and ICW3 must be reprogrammed first, in sequence. In this mode, the Interrupt Controller automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single Interrupt Controller. The AEOI mode can only be used in a master Interrupt Controller and not in a slave Interrupt Controller (on CNTRL-1 but not CNTRL-2).

10.7.3 Modes of Operation

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 being the highest). When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service Register (IS[0:7]) is set. This IS bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine. Or, if the AEOI (Automatic End of Interrupt) bit is set, this IS bit remains set until the trailing edge of the second INTA_n. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IRQ0 has the highest priority and IRQ7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode.

The Special Fully Nested Mode

This mode will be used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IRQs within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode, a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

When exiting the Interrupt Service routine, the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific End of Interrupt (EOI) command to the slave and then reading its In-Service Register and checking for zero. If it is empty, a Non-Specific EOI can be sent to the master too. If not, no EOI should be sent.

Automatic Rotation (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt will have to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2: the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0 and EOI=0) and cleared by (R=0, SL=0 and EOI=0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities. For example, if IRQ5 is programmed as the bottom priority device, IRQ6 will be the highest priority device.

The Set Priority Command is issued in OCW2 where: R=1, SL=1; L0–L2 is the binary priority level code of the bottom priority device. See the register description for the bit definitions.

Note that, in this mode, internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (R=1, SL=1, EOI=1 and L0–L2=IRQ level to receive bottom priority).

Poll Command

The Polled Mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command.

The Polled Mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table.

In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll Command.

The Poll command is issued by setting P=1 in OCW3. The Interrupt Controller treats the next I/O read pulse to the Interrupt Controller as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupts are frozen from the I/O write to the I/O read.

This mode is useful if there is a routine command common to several levels so that the INTA_n sequence is not needed (saving ROM space).

10.7.4 Cascade Mode

The Interrupt Controllers in R3210 SB are interconnected in a cascade configuration with one master and one slave. This configuration can handle up to 15 separate priority levels.

The master controls the slaves through a three-line internal cascade bus. When the master drives 010b on the cascade bus, this bus acts like a chip select to the slave controller.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master enables the corresponding slave to release the interrupt vector address during the second INTA_n cycle of the interrupt acknowledge sequence.

Each Interrupt Controller in the cascaded system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI Command must be issued twice: once for the master and once for the slave.

10.7.5 Edge- and Level-Triggered Mode

In ISA systems, this mode is programmed by using bit 3 in ICW1. With R3210 SB, this bit is disabled and a new register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2. The default programming is equivalent to programming the LTIM bit (ICW1 bit 3) to a 0 (all interrupts selected for edge triggered mode). Note that IRQ0, 1, 2, 8, and 13 cannot be programmed for level sensitive mode and cannot be modified by software.

If an ELCR bit=0, an interrupt request is recognized by a low to high transition on the corresponding IRQx input. The IRQ input can remain high without generating another interrupt.

If an ELCR bit=1, an interrupt request is recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until the falling edge of the first INTA_n. If the IRQ input goes inactive before this time, a default IRQ7 occurs when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IRQ inputs. To implement this feature, the IRQ7 routine is used for “clean up” simply executing a return instruction, thus ignoring the interrupt. If IRQ7 is needed for other purposes, a default IRQ7 can still be detected by reading the ISR. A normal IRQ7 interrupt sets the corresponding ISR bit; a default IRQ7 does not set this bit. However, if a default IRQ7 routine occurs during a normal IRQ7 routine, the ISR remains set. In this case, it is necessary to keep track of whether or not the IRQ7 routine was previously entered. If another IRQ7 occurs, it is a default.

10.7.6 Interrupt Masks

Masking on an Individual Interrupt Request Basis

Each interrupt request input can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set to a 1. Bit 0 masks IRQ0, Bit 1 masks IRQ1, and so forth. Masking an IRQ channel does not affect the other channels' operation, with one exception. Masking IRQ2 on CNTRL-1 will mask off all requests for service from CNTRL-2. The CNTRL-2 INTR output is physically connected to the CNTRL-1 IRQ2 input.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the Interrupt Controller would have inhibited all lower priority requests with no easy way for the routine to enable them.

The Special Mask Mode enables all interrupts not masked by a bit set in the Mask Register. Interrupt service routines that require dynamic alteration of interrupt priorities can take advantage of the Special Mask Mode. For example, a service routine can inhibit lower priority requests during a part of the interrupt service, then enable some of them during another part.

In the Special Mask Mode, when a mask bit is set to 1 in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupt may be selectively enabled by loading the Mask Register with the appropriate pattern.

If there is no Special Mask Mode and an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the IS bit, the interrupt controller inhibits all lower priority requests. The Special Mask Mode provides an easy way for the interrupt service routine to selectively enable only the interrupts needed by loading the Mask register.

The special Mask Mode is set by OCW3 where: SSMM=1and SMM=1, and cleared where SSMM=1 and SMM=0.

10.7.7 Reading the Interrupt Controller Status

The input status of several internal registers can be read to update the user information on the system. The Interrupt Request Register (IRR) and In-Service Register (ISR) can be read via OCW3. The Interrupt Mask Register (IMR) is read via a read of OCW1. Brief descriptions of the ISR, the IRR, and the IMR follow.

- **Interrupt Request Register (IRR):** 8-bit register which contains the status of each interrupt request line. Bits that are clear indicate interrupts that have not requested service. The Interrupt Controller clears the IRR's highest priority bit during an interrupt acknowledge cycle. (Not affected by IMR).
- **In-Service Register (ISR):** 8-bit register indicating the priority levels currently receiving service. Bits that are set indicate interrupts that have been acknowledged and their interrupt service routine started. Bits that are cleared indicate interrupt requests that have not been acknowledged, or interrupt request lines that have not been asserted. Only the highest priority

interrupt service routine executes at any time. The lower priority interrupt services are suspended while higher priority interrupts are serviced. The ISR is updated when an End of Interrupt Command is issued.

- **Interrupt Mask Register (IMR):** 8-bit register indicating which interrupt request lines are masked.

The IRR can be read when, prior to the I/O read cycle, a Read Register Command is issued with OCW3 (RR=1 and RIS=0). The ISR can be read when, prior to the I/O read cycle, a Read Register Command is issued with OCW3 (RR=1 and RIS=1).

The interrupt controller retains the ISR/IRR status read selection following each write to OCW3. Therefore, there is no need to write an OCW3 before every status read operation, as long as the current status read corresponds to the previously selected register. For example, if the ISR is selected for status read by an OCW3 write, the ISR can be read over and over again without writing to OCW3 again. However, to read the IRR, OCW3 will have to be reprogrammed for this status read prior to the OCW3 read to check the IRR. This is not true when polling mode is used. Polling Mode overrides status read when P=1 and RR=1 in OCW3.

After initialization, the Interrupt Controller is set to read the IRR. As stated, OCW1 is used for reading the IMR. The output data bus will contain the IMR status whenever I/O read is active and the address is 021h or 061h (OCW1).

10.7.8 Interrupt Steering

R3210 SB can be programmed to allow four PCI programmable interrupts (PIRQ[A:D]_n) to be internally routed to one of 11 interrupts IRQ[15,14,12:9,7:3]. PCLK is used to synchronize the PIRQx_n inputs. The PIRQx_n lines are run through an internal multiplexer that assigns, or routes, an individual PIRQx_n line to any one of 11 IRQ inputs. The assignment is programmable through the PIRQx Route Control registers. One or more PIRQx_n lines can be routed to the same IRQx input. If interrupt steering is not required, the Route Registers can be programmed to disable steering.

Bits[3:0] in each PIRQx Route Control register are used to route the associated PIRQx_n line to an internal IRQ input. Bit 7 in each register is used to disable routing of the associated PIRQx_n.

The PIRQx_n lines are defined as active low, level sensitive to allow multiple interrupts on a PCI Board to share a single line across the connector. When a PIRQx_n is routed to specify IRQ line, the software must change the IRQ's corresponding ELCR bit to level sensitive mode. This means that the selected IRQ can no longer be used by an ISA device.

10.8 LPC Interface

The LPC (Low Pin Count) interface enables a system without an ISA bus. It reduces the cost of traditional ISA-bus devices while providing the extension of legacy PC IO peripherals (such as Super IO, keyboard, mouse and Flash ROM), increasing the memory space from 16MB to 4GB to allow the BIOS size to become much bigger than 1MB and the other memory devices to exceed the traditional 16MB capacity. Software is transparent. Do not require special drivers or configuration for this interface. The LPC features are listed as below:

- LPC revision 1.0 compliant
- Supports LPC/FWH (Firmware Hub) compliant interface
- Provides the interface to LPC/FWH Flash ROM or Super IO Chip
- Supports LPC DMA
- Supports Serial IRQ
- Supports bus master mode

10.8.1 Block Diagram

Figure 10-5 contains a typical setup. In this setup, the LPC is connected through a host to a PCI or Host Bus, such as that of Intel CPUs.

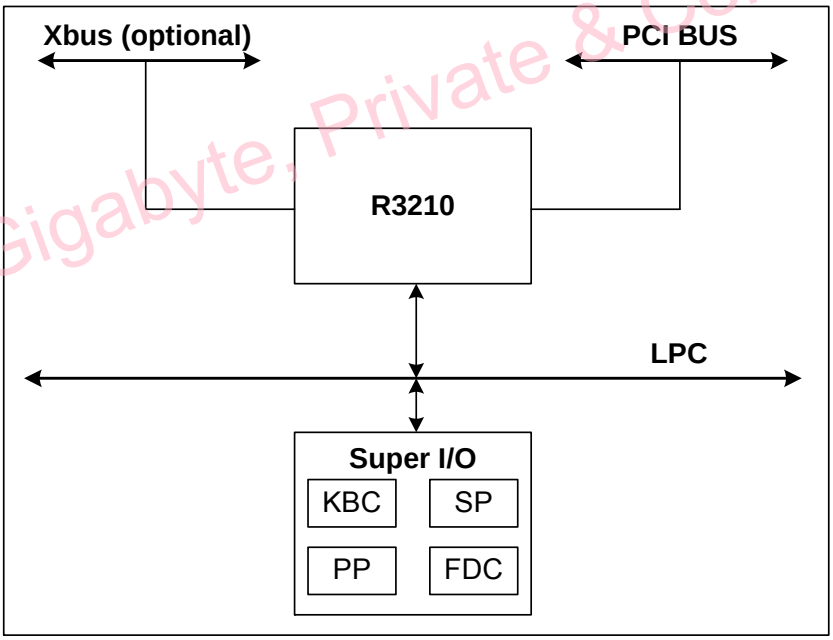


Figure 10-5. Typical Setup

10.8.2 Protocol Overview

10.8.2.1 Cycle Types

Table 10.3 shows the various types of cycles that are supported by the protocol.

Table 10.3: Cycle Types

Cycle Type	Sizes Supported	Comment
Memory Read	1 byte	Optional for both chip-sets and peripherals.
Memory Write	1 byte	Optional for both chip-sets and peripherals.
I/O Read	1 byte	Optional for peripherals.
I/O Write	1 byte	Optional for peripherals.
DMA Read	1, 2, 4 bytes	Optional for peripherals.
DMA Write	1, 2, 4 bytes	Optional for peripherals.
Bus Master Memory Read	1, 2, 4 bytes	Optional for both chip-sets and peripherals, but strongly recommended for chip-sets.
Bus Master Memory Write	1, 2, 4 bytes	Optional for both chip-sets and peripherals, but strongly recommended for chip-sets.
Bus Master I/O Read	1, 2, 4 bytes	Optional for both chip
Bus Master I/O Write	1, 2, 4 bytes	Optional for both chip

The following rules must be followed:

- The host will support all cycle types, unless otherwise indicated.
- Peripherals may implement cycles as needed. For example, a peripheral may be chosen to implement just I/O cycles, not memory, DMA, or bus master cycles.
- Peripherals must not attempt bus master cycles that are not supported by the chip-set. For example, if the chip-set does not support bus master I/O cycles, the peripheral must not attempt those cycles.
- Peripherals must ignore cycles that they do not support.

10.8.2.2 Cycle Overview

Data transfers on the LPC bus are serialized over a 4-bit bus. The general characteristics of this bus are:

- One control line, called LFRAME_n, which is used by the host to start or stop transfers. No peripherals drive this signal.
- The LAD[3:0] bus, which communicates information serially. The information conveyed is cycle type, cycle direction, chip selection, address, data, and wait states.
- Side-band signals, optionally implemented, which convey interrupts and power management features. These signals are the same as many signals found on current motherboard implementations.

The general flow of cycles is as follows:

1. A cycle is started by the host when it drives LFRAME_n to be active and puts appropriate information on the LAD[3:0] signal lines.
2. The host drives information relative to the cycle, such as address, or DMA channel number, or bus master grant. For DMA and target cycles, the host also drives cycle type (memory or I/O), read/write direction, and size of the transfer.
3. The host optionally drives data, and turns the bus around to monitor the peripheral for completion of the cycle.
4. The peripheral indicates completion of the cycle by driving appropriate values on the LAD[3:0] signal lines, and potentially drives data.
5. The peripheral turns the bus around to the host, ending the cycle.

For bus master cycles, there are small changes to this protocol, as the bus master must drive control and address information to the host, and the host is responsible for ending the cycle, but in general, the flow is the same.

10.8.3 Target Overview

10.8.3.1 Memory Cycles

In these cases, memory read or write cycles are intended for memory-mapped devices. The Sync time will depend on the speed of the device.

The ADDR field is full 32 bits, and transmitted with the most significant nibble first. Although a full 32 bits of addressing is supported, a memory device will typically support much less than this. It can ignore the address bits which it is capable of decoding.

10.8.3.2 I/O Cycles

In these cases, I/O read or write cycles are intended for the peripheral. These will generally be used for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times. Data transfers are assumed to be exactly 1 byte. The host is responsible for breaking up larger data transfers into 8-bit cycles.

10.8.4 DMA Protocol

DMA on LPC is handled through the use of the LDRQ_n lines from peripherals and special encodings on LAD[3:0] from the host. Single, demand, verify, and increment modes are supported on the LPC interface. Block, decrement, and cascade modes are not supported. Channel 0 - 3 are 8-bit channels. Channel 5 - 7 are 16-bit channels. Channel 4 is reserved as a generic bus master request (see section 7).

A new 32-bit transfer mode is supported on the LPC interface, which can be used to transfer multiple bytes from an 8- or 16-bit channel per request for faster throughput.

10.8.5 Bus Master Protocol

The LPC interface does not support cascaded ISA master mode access on DMA channels. Bus master accesses are performed through a reserved encoding on the LDRQ_n signal line of ‘100b’. By using this reserved encoding, a peripheral is able to create any number of bus masters, and is not limited to the number of DMA channels in the system.

10.8.5.1 Cycle Formats and Timings

Bus master START fields are associated with either Bus Master 0 (‘0010b’) or Bus Master 1 (‘0011b’). At this time, there are only two bus masters supported on the LPC interface. After sending this field, the host performs a TAR to transfer control to the peripheral.

10.9 FIFO UART

The R3210 integrates an improved version of Universal Asynchronous Receiver/Transmitter (UART). The internal 16-byte FIFOs are activated and allowed to be stored in both receive and transmit modes. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operations. Reported status information includes the types and conditions of the transfer operations being performed by the FIFO UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

- Programmable word length, stop bit and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Two 16-byte FIFOs

The UART clock is 1.8432MHz. The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link. The reference table of baud rates and 16x clock is as followed:

Baud Rate	1.8432 MHz Crystal Decimal Divisor for 16x Clock
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3

10.9.1 Transmit Operation

Transmission is initiated by writing the data to be sent to the TX Holding Register or to the TX FIFO (if enabled). The data will then be transferred to the TX Shift Register together with a start bit and parity and stop bits as determined by the Line Control Register. The bits to be transmitted are then shifted out of the TX Shift Register with the output from the baud rate generator as the clock.

If enabled, an interrupt will be generated when the TX Holding Register becomes empty.

When FIFOs are enabled (i.e. Bit 0 of the FIFO Control Register is set), the FIFO UART can store up to 16 bytes of data for transmission at a time. Transmission will continue until the TX FIFO is empty. The FIFO readiness to accept more data is indicated by TXRDY_n or, if the transfer is interrupt driven, by INTR.

10.9.2 Receive Operation

Data is sampled into the RX Shift Register with either the baud rate generator or RCLK. A filter is used to remove spurious inputs that last for less than two periods of the clock.

When the complete word has been clocked into the receiver, the data bits are transferred to the RX Buffer Register or to the RX FIFO (if enabled) to be read by the CPU. The receiver also checks for a stop bit and for correct parity as determined by the Line Control Register.

If enabled, an interrupt will be generated when data has been transferred to the RX Buffer Register. Interrupts can also be generated for incorrect parity or a missing stop bit (frame error).

When FIFOs are enabled (i.e. Bit 0 of the FIFO Control Register is set), the FIFO UART can store up to 16 bytes of received data at a time. Depending on the selected mode, either RXRDY_n of INTR will go active to indicate that it is available when the RX FIFO contains 1, 4, 8 or 14 bytes of data.

10.9.3 MODEM Control Lines

The output Modem Control lines RTS_n, DTR_n, OUT1_n, and OUT2_n can be set or cleared by writing to the MODEM Control Register.

The current status of the input Modem Control lines DCD_n, RI_n, DSR_n and CTS_n can be read from the Modem Status Register. Bit 2 of this register will be set if the RI_n line has been changed from low to high since the register was last read.

If enabled, an interrupt will be generated when any of DSR_n, CTS_n, RI_n or DCD_n is asserted.

10.9.4 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR0 = 1 and IER0 = 1), RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR = 6), as before, has higher priority than the received data available (IIR = 04)

D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

- at least one character is in the FIFO
- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed and the second one is included in this time delay).
- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

The maximum time between a received character and a timeout interrupt will be 160 ms at 300 baud with a 12-bit receive character (i.e., 1 Start, 8 Data, 1 Parity and 2 Stop Bits).

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred, it is cleared and the timer is reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0 = 1 and IER1= 1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first transmitter interrupt after FCR0 is changed will be immediate if it is enabled. Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

10.9.5 FIFO Polled Mode Operation

With FCR0 = 1, resetting IER0, IER1, IER2, IER3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMIT-TER status via the LSR, as stated previously:

LSR0 will be set as long as there is one byte in the RCVR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as in the interrupt mode. The IIR is not affected since IER2 = 0.

LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

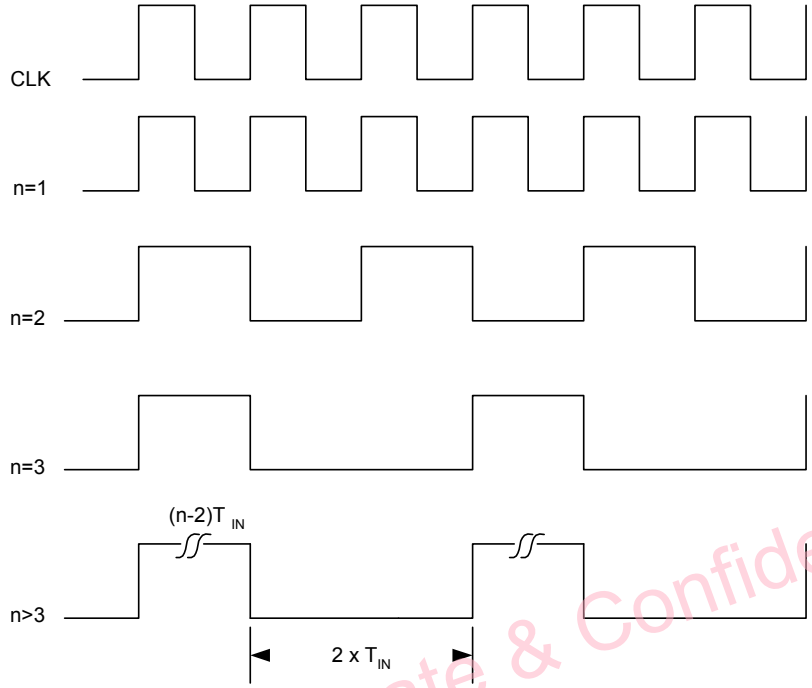
LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode. However, the RCVR and XMIT FIFOs are still fully capable of holding characters.

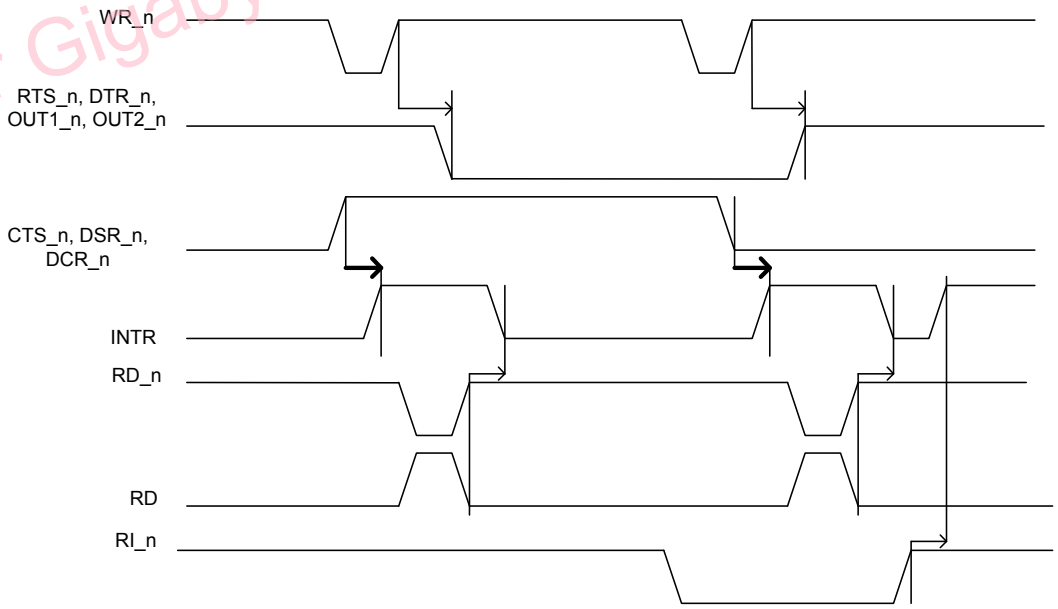
10.9.6 Timing Waveforms

The following timing diagrams are given as a guide when inputs to the FIFO UART must be valid, and when outputs are valid. Many of the signals are synchronized with XIN. The actual set-up and delay time will also depend on the technology used for the FIFO UART.

Baud Rate Generator Output



MODEM Control Timig



10.10 X-Bus Interface

The R3210 provides an X-bus interface to connect to system boot flash ROM or DOC (Disk On Chip).

- Supports 8-/16-bit data width
- Provides ROMCS_n for boot from X-bus Flash ROM
- Supports from 64 Kbytes to Max. 8 Mbytes ROM space addressing

10.11 GPIO Interface

59 GPIO pins are provided by the R3210 for general usage in the system. All GPIO pins are independent and can be configured as inputs or outputs, with or without pull-up/pull-down resistors.

GPIO pin list table

GPIO Number	PIN Number	Symbol	Note
0	18	LAD0/GPIO0	LPC Bus Interface
1	19	LAD1/GPIO1	LPC Bus Interface
2	20	LAD2/GPIO2	LPC Bus Interface
3	22	LAD3/GPIO3	LPC Bus Interface
4	23	LFRAME_n/GPIO4	LPC Bus Interface
5	24	LDRQ_n/GPIO5	LPC Bus Interface
6	25	SERIRQ/GPIO6	LPC Bus Interface
7	120	SIN/GPIO7	FIFO UART
8	121	SOUT/GPIO8	FIFO UART
9	114	RTS_n/TDO /GPIO9	FIFO UART
10	112	DTR_n/GPIO10	FIFO UART
11	115	CTS_n/TMS/GPIO11	FIFO UART
12	117	DSR_n/TCK/GPIO12	FIFO UART
13	118	DCD_n/TDI/GPIO13	FIFO UART
14	113	RI_n/GPIO14	FIFO UART
15	29	RTCAS/GPIO15	External RTC Interface
16	30	RTCRD/GPIO16	External RTC Interface
17	31	RTCWR/GPIO17	External RTC Interface
18	32	IRQ8_n/GPIO18	External RTC Interface
19	158	INTA_n/GPIO19	PCI Bus Interface
20	157	INTB_n/GPIO20	PCI Bus Interface
21	156	INTC_n/GPIO21	PCI Bus Interface
22	155	INTD_n/GPIO22	PCI Bus Interface
23	1	PREQ_n0/GPIO23	PCI Bus Interface
24	216	PREQ_n1/GPIO24	PCI Bus Interface
25	215	PREQ_n2/GPIO25	PCI Bus Interface
26	214	PGNT_n0/GPIO26	PCI Bus Interface
27	213	PGNT_n1/GPIO27	PCI Bus Interface
28	212	PGNT_n2/GPIO28	PCI Bus Interface
29	91	SA13/GPIO29	XD Bus Address Bus
30	92	SA14/GPIO30	XD Bus Address Bus
31	93	SA15/GPIO31	XD Bus Address Bus
32	94	SA16/GPIO32	XD Bus Address Bus
33	95	SA17/GPIO33	XD Bus Address Bus
34	97	SA18/GPIO34	XD Bus Address Bus
35	98	SA19/GPIO35	XD Bus Address Bus
36	100	SA20/GPIO36	XD Bus Address Bus
37	101	SA21/GPIO37	XD Bus Address Bus
38	102	SA22/GPIO38	XD Bus Address Bus
39	103	SA23/GPIO39	XD Bus Address Bus
40	128	TXC0/GPIO40	MII Interface
41	129	TXD0_0/GPIO41	MII Interface

42	130	TXD0_1/GPIO42	MII Interface
43	131	TXD0_2/GPIO43	MII Interface
44	132	TXD0_3/GPIO44	MII Interface
45	134	TXEN0/GPIO45	MII Interface
46	127	RXC0/GPIO46	MII Interface
47	122	RXDV0/GPIO47	MII Interface
48	123	RXD0_0/GPIO48	MII Interface
49	124	RXD0_1/GPIO49	MII Interface
50	125	RXD0_2/GPIO50	MII Interface
51	126	RXD0_3/GPIO51	MII Interface
52	135	COL0/GPIO52	MII Interface
53	108	SPEAKER/GPIO53	Speaker Output
54	111	A20GATE_n/GPIO54	Address Bit 20 Mask
55	109	KBRST_n/GPIO55	Keyboard Reset
56	27	CLK25MOUT/GPIO56	25MHz Clock output
57	106	XCS1_n/GPIO57	XBUS Chip Select 1
58	107	XCS2_n/GPIO58/CLK14M	XBUS Chip Select 2/CLK14M

11. Register Description

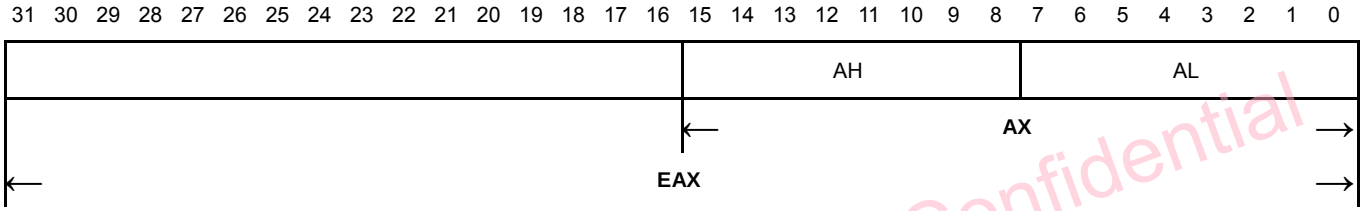
In this chapter, we give the detailed descriptions for each register in R3210 RISC Microprocessor.

11.1 Core Registers

11.1.1 General-Purpose Registers

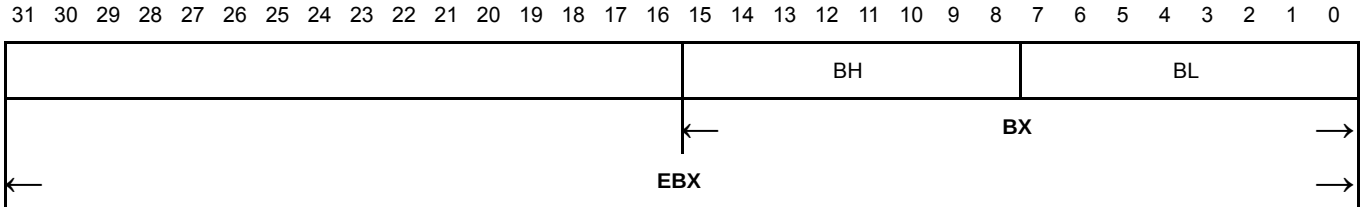
The 32-bit general-purpose data registers EAX, EBX, ECX, EDX, ESI, EDI, EBP and ESP are provided for holding the Operands for logical and arithmetic operations, Operands for address calculations or Memory pointers.
As shown below, the lower 16 bits of the general-purpose registers map directly to the register set found in the 8086 and Intel 286 processors and can be referenced with the names AX, BX, CX, DX, BP, SP, SI, and DI. Each of the lower two bytes of the EAX, EBX, ECX, and EDX registers can be referenced by the names AH, BH, CH, and DH (high bytes) and AL, BL, CL, and DL (low bytes).

Register Name: EAX
Reset Value: --------



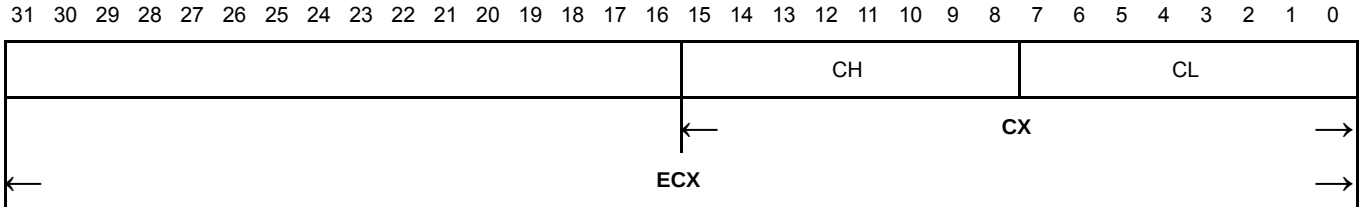
Bit	Name	Attribute	Description
31-0	EAX	R/W	The EAX registers are available for general storage of operands, results and pointers. For special purpose, the EAX holds the accumulator's operands or results data.

Register Name: EBX
Reset Value: --------



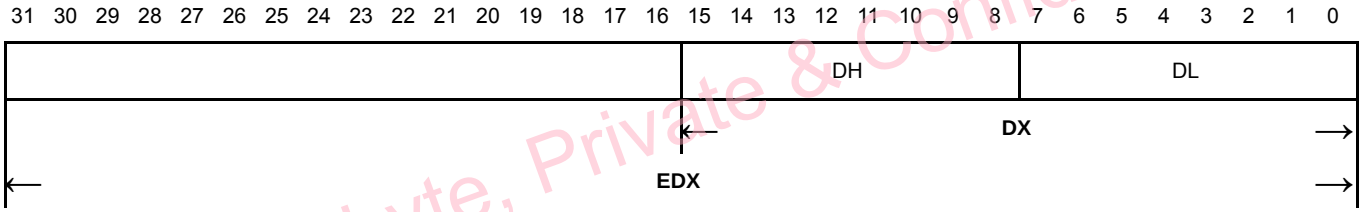
Bit	Name	Attribute	Description
31-0	EBX	R/W	The EBX registers are available for general storage of operands, results and pointers. For special purpose, the EBX holds a pointer which points to data in the DS segment.

Register Name: ECX
Reset Value: --------



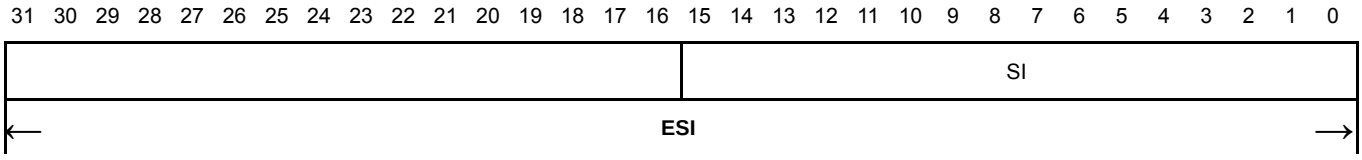
Bit	Name	Attribute	Description
31-0	ECX	R/W	The ECX registers are available for general storage of operands, results and pointers. For special purpose, the ECX holds a string pointer or the counter values of loop operations.

Register Name: EDX
Reset Value: --------



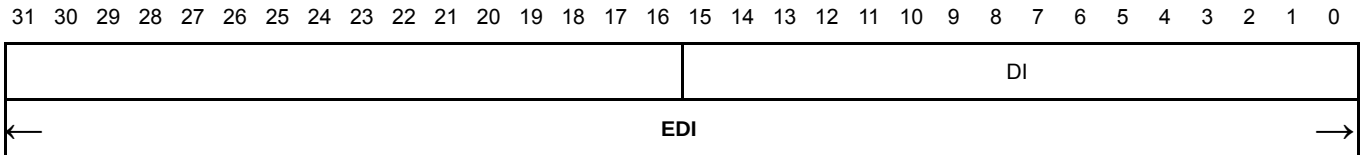
Bit	Name	Attribute	Description
31-0	EDX	R/W	The EDX registers are available for general storage of operands, results and pointers. For special purpose, the EDX holds an I/O pointer.

Register Name: ESI
Reset Value: --------



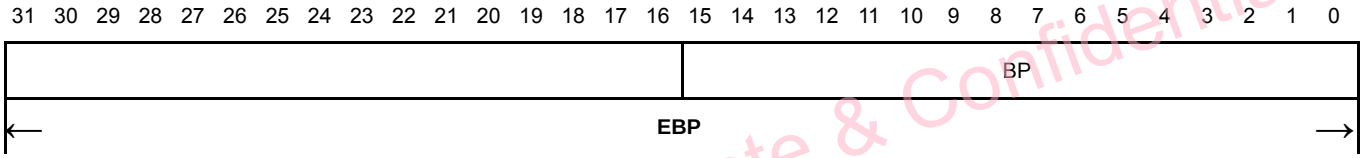
Bit	Name	Attribute	Description
31-0	ESI	R/W	Pointer to data in the segment pointed to by the DS register; source pointer for string operations.

Register Name: EDI
Reset Value: --------



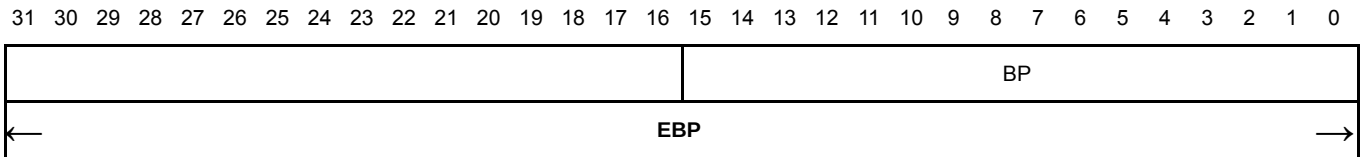
Bit	Name	Attribute	Description
31-0	EDI	R/W	Pointer to data (or destination) in the segment pointed to by the ES register; destination pointer for string operations.

Register Name: EBP
Reset Value: --------



Bit	Name	Attribute	Description
31-0	EBP	R/W	Stack pointer (in the SS segment).

Register Name: ESP
Reset Value: --------



Bit	Name	Attribute	Description
31-0	EBP	R/W	Pointer to data on the stack (in the SS segment).

11.1.2 Segment Registers

Six 16-bit segment registers hold segment selector values identifying the currently addressable memory segments. In protected mode, each segment may range in size from one byte up to the entire linear and physical address space of the machine, which is 4 Gbytes (2^{32} bytes). In real address mode, the maximum segment size is fixed at 64 Kbytes (2^{16} bytes).

Register Name: Code segment Register (CS)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS															

Bit	Name	Attribute	Description
15-0	CS	R/W	The Code Segment Register – CS holds the 16-bit code segment selector which points to the code segment.

Register Name: Stack segment Register (SS)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS															

Bit	Name	Attribute	Description
15-0	SS	R/W	The Stack Segment Register –SS holds the 16-bit stack segment selector.

Register Name: Data segment Register (DS)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS															

Bit	Name	Attribute	Description
15-0	DS	R/W	The Data Segment Register – DS holds the data segment selector.

Register Name: Data segment Register (ES)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES															

Bit	Name	Attribute	Description
15-0	ES	R/W	The Data Segment Register – ES holds the data segment selector.

Register Name: Data segment Register (FS)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS															

Bit	Name	Attribute	Description
15-0	FS	R/W	The Data Segment Register – FS holds the data segment selector.

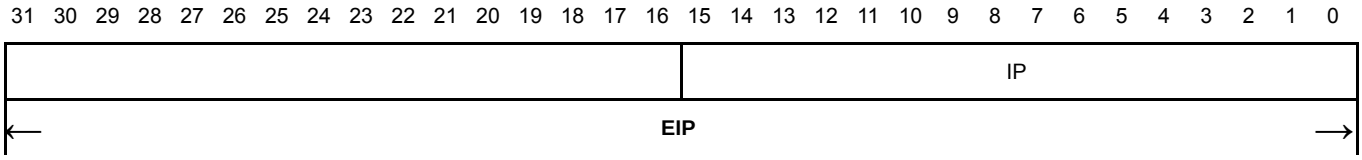
Register Name: Data segment Register (GS)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GS															

Bit	Name	Attribute	Description
15-0	GS	R/W	The Data Segment Register – GS holds the data segment selector.

11.1.3 Instruction Pointer Register

Register Name: Instruction Pointer (EIP)
Reset Value: --------

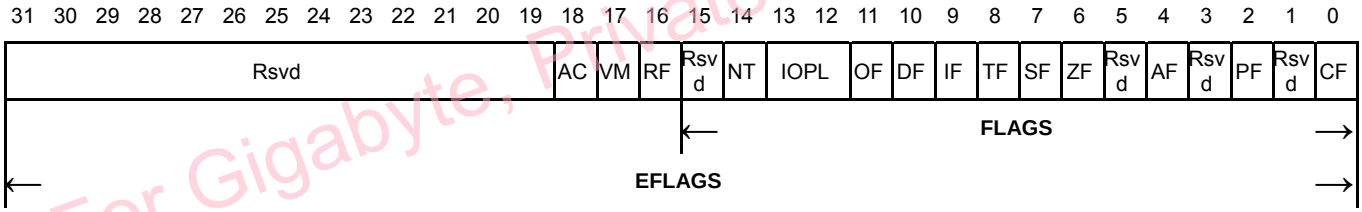


The instruction pointer is a 32-bit register named EIP.

Bit	Name	Attribute	Description
31-0	EIP	R/W	EIP holds the offset of the next instruction to be executed. The offset is always relative to the base of the code segment (CS). The lower 16 bits (bits 0-15) of the EIP contain the 16-bit instruction pointer named IP, which is used for 16-bit addressing.

11.1.4 Flags Register

Register Name: Flags Register (EFLAGS)
Reset Value: --------



The flags register is a 32-bit register named EFLAGS. The defined bits and bit fields within EFLAGS control certain operations and indicate the status of the R3210 RISC processor core. The lower 16 bits (bits 0-15) of EFLAGS contain the 16-bit register named FLAGS, which is most useful when the processor executes 8086 and 80286 codes.

EFLAGS bits 1, 3, 5, 15 and 19-31 are “undefined”. When these bits are stored during interrupt processing or with a PUSHF instruction (push flags onto stack), a one is stored in bit 1 and zeros in bit 3, 5, 15 and 19-31.

Bit	Name	Attribute	Description
31-19	Rsvd	RO	Reserved.

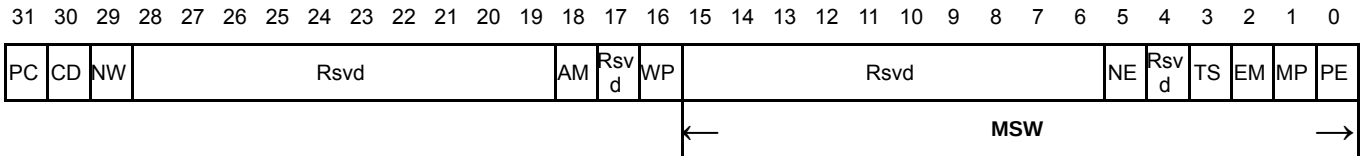
<table>
<tr>
<td>18</td>
<td>AC</td>
<td>R/W</td>
<td>Alignment Check.
The AC bit enables the generation of faults if a memory reference is to a misaligned address. Alignment faults are enabled when AC is set to 1. A misaligned address is a word access to an odd address, a dword access to an address that is not on a dword boundary, or an 8-byte reference to an address that is not on a 64-bit word boundary.
Alignment faults are only generated by programs running at privilege level 3. The AC bit setting is ignored at privilege levels 0, 1 and 2. Note that references to the descriptor tables (for selector loads) or the task state segment (TSS) are implicitly level 0 references even if the instructions causing the reference are executed at level 3. Alignment faults are reported through interrupt 17, with an error code of 0. Table 2.1 gives the alignments required for the R3210 RISC processor core data types.
<table>
<tr><th>Memory Access</th><th>Alignment (Byte Boundary)</th></tr>
<tr><td>Word</td><td>2</td></tr>
<tr><td>Dword</td><td>4</td></tr>
<tr><td>Selector</td><td>2</td></tr>
<tr><td>48-bit Segmented Pointer</td><td>4</td></tr>
<tr><td>32-bit Flat Pointer</td><td>4</td></tr>
<tr><td>32-bit Segmented Pointer</td><td>2</td></tr>
<tr><td>48-bit “Pseudo-Descriptor”</td><td>4</td></tr>
</table>
Note:
Several instructions on the R3210 RISC processor core generate misaligned references, even if their memory address is aligned. For example, on this processor core, the SGDT/SIDT (store global/internet descriptor table) instruction reads/writes two bytes, and then reads/writes four bytes from a “pseudo-descriptor” at the given address. The R3210 RISC processor core will generate misaligned references unless the address is on a 2 mod 4 boundary. The R3210 RISC processor core will not cause any AC faults if the effective address given in the instruction has the proper alignment.</td>
</tr>
<tr>
<td>17</td>
<td>VM</td>
<td>R/W</td>
<td>Virtual 8086 Mode.
The VM bit provides virtual 8086 mode within protected mode. If set while the R3210 RISC processor core is in protected mode, the processor core will switch to virtual 8086 operation, handling segment loads as the 8086 does, but generating exception 13 faults on privileged opcodes. The VM bit can be set only in protected mode, by the IRET instruction (if the current privilege level = 0) and by task switches at any privilege level. The VM bit is unaffected by POPF. PUSHF always pushes a 0 in this bit, even if executing in virtual 8086 mode. The EFLAGS image pushed during interrupt processing or saved during task switches will contain a 1 in this bit if the interrupted code was executing as a virtual 8086 task.</td>
</tr>
<tr>
<td>16</td>
<td>RF</td>
<td>R/W</td>
<td>Resume Flag.
The RF flag is used in conjunction with the debug register breakpoints. It is checked at instruction boundaries before breakpoint processing. When RF is set, it causes any debug fault to be ignored on the next instruction. RF is then automatically reset at the successful completion of every instruction (no faults are signaled) except the IRET instruction, the POPF instruction, and JMP, CALL, and INT instructions causing a task switch. These instructions set RF to the value specified by the memory image. For example, at the end of the breakpoint service routine, the IRET instruction can pop an EFLAG image having the RF bit set and resume the program’s execution at the breakpoint address without generating another breakpoint fault on the same location.</td>
</tr>
<tr>
<td>15</td>
<td>Rsvd</td>
<td>RO</td>
<td>Reserved.</td>
</tr>
<tr>
<td>14</td>
<td>NT</td>
<td>R/W</td>
<td>Nested Task.
This flag applies to Protected Mode. NT is set to indicate that the execution of this task is nested within another task. If set, it indicates that the current nested task’s Task State Segment (TSS) has a valid back link to the previous task’s TSS. This bit is set or reset by control transfers to other tasks. The value of NT in EFLAGS is tested by the IRET instruction to determine whether to do an inter-task return or an intra-task return. A POPF or an IRET instruction will affect the setting of this bit according to the image popped, at any privilege level.</td>
</tr>
</table>

13-12	IOPL	R/W	Input/Output Privilege Level. This two-bit field applies to Protected Mode. IOPL indicates the numerically maximum CPL (current privilege level) value permitted to execute I/O instructions without generating an exception 13 faults or consulting the I/O Permission Bitmap. It also indicates the maximum CPL value allowing alteration of the IF (INTR Enable Flag) bit when new values are popped into the EFLAG register. POPF and IRET instructions can alter the IOPL field when executed at CPL = 0. Task switches can always alter the IOPL field when the new flag image is loaded from the incoming task's TSS.
11	OF	R/W	Overflow Flag. OF is set if the operation resulted in signed overflow. Signed overflow occurs when the operation resulted in carry/borrow into the sign bit (high-order bit) of the result but did not result in a carry/borrow out of the high-order bit, or vice-versa. For 8-, 16- and 32-bit operations, OF is set according to overflow at bit 7, 15 and 31 respectively.
10	DF	R/W	Direction Flag. DF defines whether ESI and/or EDI register postdecrement or postincrement during the string instructions. Postinstruction occurs if DF is reset. Post decrement occurs if DF is set.
9	IF	R/W	INTR Enable Flag. The IF flag, when set, allows recognition of external interrupts signaled on the INTR pin. When IF is reset, external interrupts signaled on the INTR are not recognized. IOPL indicates the maximum CPL value allowing alteration of the IF bit when new values are popped into EFLAGS or FLAGS.
8	TF	R/W	Trap Enable Flag. TF controls the generation of exception 1 trap when single-stepping through code. When TF is set, the R3210 RISC processor core generates an exception 1 trap after the next instruction is executed. When TF is reset, exception 1 traps occur only as a function of the breakpoint addresses loaded into debug registers DR[0:3].
7	SF	R/W	Sign Flag. SF is set if the high-order bit of the result is set, it is reset otherwise. For 8-, 16- and 32-bit operations, SF reflects the state of bit 7, 15 and 31 respectively.
6	ZF	R/W	Zero Flag. ZF is set if all bits of the result are 0. Otherwise it is reset.
5	Rsvd	RO	Reserved.
4	AF	R/W	Auxiliary Carry Flag. The Auxiliary Flag is used to simplify the addition and subtraction of packed BCD quantities. AF is set if the operation results in a carry out of bit 3 (addition) or a borrow into bit 3 (subtraction). Otherwise AF is reset. AF is affected by carry out of, or borrow into bit 3 only, regardless of overall operand length: 8, 16 or 32 bits.
3	Rsvd	RO	Reserved.
2	PF	R/W	Parity Flags. PF is set if the low-order eight bits of the operation contain an even number of "1"s (even parity). PF is reset if the low-order eight bits have odd parity. PF is a function of only the low-order eight bits, regardless of operand size.
1	Rsvd	RO	Reserved.
0	CF	R/W	Carry Flag. CF is set if the operation results in a carry out of (addition), or a borrow into (subtraction) the high-order bit. Otherwise CF is reset. For 8-, 16- or 32-bit operations, CF is set according to carry/borrow at bit 7, 15 or 31 respectively.

11.1.5 Control Registers

Register Name: Control Register 0 (CR0)

Reset Value: --------



CR0 contains 10 bits for control and status purposes. The function of the bits in CR0 can be categorized as follows:

R3210 RISC Processor Core Operating Modes: PG, PE (Table 5.2)

On-Chip Cache Control Modes: CD, NW (Table 5.3)

On-Floating Point Unit Control: TS, EM, MP, NE (Table 5.4)

Alignment Check Control: AM

Supervisor Write Protect: WP

Table 11.2. R3210 RISC Processor Core Operating Modes

PG	PE	Mode
0	0	REAL Mode. Exact 8086 semantics, with 32-bit extensions available with prefixes.
0	1	Protected Mode. Exact 80286 semantics, plus 32-bit extensions through both prefixes and "default" prefix setting associated with code segment descriptors. Also, a submode is defined to support a virtual 8086 within the context of the extended 80286 protection model.
1	0	UNDEFINED. Loading CR0 with this combination of PG and PE bits will raise a GP fault with error code 0.
1	1	Paged Protected Mode. All the facilities of Protected mode, with paging enabled underneath segmentation.

Table 11.3 On-Chip Cache Control Modes

CD	NW	Operating Mode
1	1	Cache fills disabled, write-through and invalidates disabled.
1	0	Cache fills disabled, write-through and invalidates enabled.
0	1	INVALID. If CR0 is loaded with this configuration of bits, a GP fault with error code is raised.
0	0	Cache fills enabled, write-through and invalidates enabled.

Table 11.4 R3210 RISC Processor Core Floating Point Instruction Control

CR0 BIT			Instruction Type	
EM	TS	MP	Floating-Point	Wait
0	1	0	Trap 7	Execute
0	1	1	Trap 7	Trap 7
1	0	0	Trap 7	Execute
1	0	1	Trap 7	Execute
1	1	0	Trap 7	Execute
1	1	1	Trap 7	Trap 7

The low-order 16 bits of CR0 are also known as the Machine Status Word (MSW), for compatibility with the 80286 protected mode. LMSW and SMSW (load and store MSW) instructions are taken as special aliases of the load and store CR0 operations, where only the low-order 16 bits of CR0 are involved. The LMSW and SMSW instructions in the R3210 RISC processor core work in an identical fashion to the LMSW and SMSW instructions in the 80286 (i.e., they only operate on the low-order 16 bits of CR0 and ignore the new bits). New R3210 RISC processor core operating systems should use the MOV CR0, Reg instruction.

The defined CR0 bits are described below.

Bit	Name	Attribute	Description
31	PG	R/W	Paging Enable. The PG bit is used to indicate whether paging is enabled (PG = 1) or disabled (PG = 0). See Table 5.2.
30	CD	R/W	Cache Disable. The CD bit is used to enable the on-chip cache. When CD = 1, the cache will not be filled on cache misses. When CD = 0, cache fills may be performed on misses. See Table 5.3. The state of the CD bit, the cache enable input pin (KEN_n), and the relevant page cache disable (PCD) bit determine if a line read in response to a cache miss will be installed in the cache. A line is installed in the cache only if CD = 0 and KEN_n and PCD are both zero. The relevant PCD bit comes from either the page table entry, page directory entry or control register 3. Refer to Section 5.6 for more details on page cacheability. CD is set to one after RESET.
29	NW	R/W	Not Write-Through. The NW bit enables on-chip cache write-through and write-invalidate cycles (NW = 0). When NW = 0, all writes, including cache hits, are sent out to the pins. Invalidate cycles are enabled when NW = 0. During an invalidate cycle, a line will be removed from the cache if the invalidate address hits in the cache. See Table 5.3. When NW = 1, write-through and write-invalidate cycles are disabled. A write will not be sent to the pins if the write hits in the cache. With NW = 1, the only write cycles that reach the external bus are cache misses. Write hits with NW = 1 will never update main memory. Invalidate cycles are ignored when NW = 1.
28-19	Rsvd	RO	Reserved.
18	AM	R/W	Alignment Mask. The AM bit controls whether the alignment check (AC) bit in the flag register (EFLAGS) can allow an alignment fault. AM = 0 disables the AC bit. AM = 1 enables the AC bit. AM = 0 is the 386 microprocessor compatible mode. The 386 microprocessor software may load incorrect data into the AC bit in the EFLAGS register. Setting AM = 0 will prevent AC faults from occurring before the R3210 RISC processor core has created the AC interrupt service routine.
17	Rsvd	RO	Reserved.
16	WP	R/W	Write Protect. WP protects read-only pages from supervisor write access. The 386 microprocessor allows a read-only page to be written from privilege level 0-2. The R3210 RISC processor core is compatible with the 386 microprocessor when WP = 0. WP = 1 forces a fault on a write to a read-only page from any privilege level. Operating systems with Copy-on-Write features can be supported with the WP bit. Refer to Section 5.5.3 for further details on use of the WP bit.
15-6	Rsvd	RO	Reserved.
5	NE	R/W	Numerics Exception. For the R3210 RISC processor core, interrupt 7 will be generated upon encountering any floating-point instruction regardless of the value of the NE bit. It is recommended that NE = 1 for normal operation of the R3210 RISC processor core.
4	Rsvd	RO	Reserved.
3	TS	R/W	Task Switch. The TS bit is set whenever a task switch operation is performed. Execution of floating point instructions with TS = 1 will cause a “device not available” (DNA) fault (trap vector 7). With MP = 0, the value of the TS bit is a “don’t care” for the WAIT instructions, i.e., these instructions will not generate trap 7.

2	EM	R/W	Emulate Coprocessor. The EM bit should be set to one for the R3210 RISC processor core. This will cause the processor core to trap via interrupt vector 7 (Device Not Available) to a software exception handler whenever it encounters a floating-point instruction. If EM bit is 0, the system will hang.
1	MP	R/W	Monitor Coprocessor. For normal operation of the R3210 RISC processor core, it is required to set this bit as zero (MP = 0). The MP bit is used in conjunction with the TS bit to determine if WAIT instructions should trap. For MP = 0, the value of TS is a “don’t care” for these type of instructions.
0	PE	R/W	Protection Enable. The PE bit enables the segment based protection mechanism. If PE = 1, protection is enabled. When PE = 0, the R3210 RISC processor core operates in REAL mode, with segment based protection disabled, and addresses formed as in an 8086. Refer to Table 5.2.

Register Name: Control Register 1 (CR1)

Reset Value: --------

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR1																															

Bit	Name	Attribute	Description
31-0	CR1	--	Control Register 1. CR1 is reserved for use in the oncoming RDC microprocessor.

Register Name: Control Register 2 (CR2)

Reset Value: --------

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR2																															

Bit	Name	Attribute	Description
31-0	CR2	R/W	Control Register 2. (Page Fault Linear Address Register) CR2 holds the 32-bit linear address that caused the last page fault detected. The error code pushed onto the page fault handler’s stack when it is invoked provides additional status information on this page fault.

Register Name: Control Register 3 (CR3)
Reset Value: --------

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDBR																				Rsvd							PCD	PWT	Rsvd		

CR3 contains the physical base address of the page directory table. The page directory is always page aligned (4 Kbyte-aligned).

In the R3210 RISC processor core, CR3 contains two bits, page write-through (PWT, bit 3) and (PCD, bit 4), which control page cacheability. The page table entry (PTE) and page directory entry (PDE) also contain PWT and PCD bits. When a page is accessed in external memory, the state of PWT and PCD are driven out on the PWT and PCD pins. The source of PWT and PCD can be CR3, the PTE or the PDE. PWT and PCD are sourced from CR3 when the PDE is being updated. When paging is disabled (PG = 0 in CR0), PCD and PWT are assumed to be 0, regardless of their state in CR3.

A task switch through a task state segment (TSS) which changes the values in CR3, or an explicit load into CR3 with any value, will invalidate all cached page table entries in the translation look aside buffer (TLB).

The page directory base address in CR3 is a physical address. The page directory can be paged out while its associated task is suspended, but the operating system must ensure that the page directory is resident in physical memory before the task is dispatched. The entry in the TSS for CR3 has a physical address, with no provision for a present bit. This means that the page directory for a task must be resident in physical memory. The CR3 image in a TSS must point to this area, before the task can be dispatched through its TSS.

Bit	Name	Attribute	Description
31-12	PDBR	R/W	Page Directory Base Register. The page directory is always page aligned (4 Kbyte-aligned). This alignment is enforced by the only storing bits 20-31 in CR3.
11-5	Rsvd	RO	Reserved.
4	PCD	R/W	Page Cache Disable.
3	PWT	R/W	Page Write-Through.
2-0	Rsvd	RO	Reserved.

11.1.6 System Address Registers

Four special registers are defined to reference the tables or segments supported by the R3210 RISC processor core protection model. These tables or segments are:

GDT (Global Descriptor Table)
IDT (Interrupt Descriptor Table)
LDT (Local Descriptor Table)
TSS (Task State Segment)

The address of these tables and segments are stored in special registers, the System Address and System Segment Registers. These registers are named GDTR, IDTR, LDTR and TR respectively.

Register Name: Global Descriptor Table Register (GDTR)
Reset Value: ----------

47 ... 16	15 ... 0
GLBA	GLIMT

The GDTR holds the 32-bit linear base address and 16-bit limit of the GDT, respectively.

Since the GDT segments are global to all tasks in the system, the GDT are defined by 32-bit linear addresses (subject to page transition if paging is enabled) and 16-bit limit values.

Bit	Name	Attribute	Description
47-16	GLBA	R/W	Linear Base addresses of GDT. This field saves the 32-bit linear address of Global Descriptor Table.
15-0	GLMT	R/W	Limit of GDT. This field saves the 16-bit limit values of Global Descriptor Table.

Register Name: Interrupt Descriptor Table Register (IDTR)
Reset Value: ----------

47 ... 16	15 ... 0
ILBA	ILIMT

The IDTR holds the 32-bit linear base address and 16-bit limit of the IDT, respectively.

Since the IDT segments are global to all tasks in the system, the IDT are defined by 32-bit linear addresses (subject to page transition if paging is enabled) and 16-bit limit values.

Bit	Name	Attribute	Description
47-16	ILBA	R/W	Linear Base addresses of IDT. This field saves the 32-bit linear address of Interrupt Descriptor Table.
15-0	ILMT	R/W	Limit of IDT. This field saves the 16-bit limit values of Interrupt Descriptor Table.

Register Name: Local Descriptor Table Register (LDTR)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDTS															

The LDTR holds the 16-bit selector for the LDT descriptor.

Since the LDT segment is task specific segment, the LDT are defined by selector value stored in the system segment register.

Bit	Name	Attribute	Description
16-0	LDTS	R/W	Selector of LDT descriptor. The LDTR holds the 16-bit selector for the LDT descriptor.

Register Name: Task State Segment Register (TSSR)
Reset Value: ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSSS															

The TSSR holds the 16-bit selector for the TSS descriptor.

Since the TSS segment is task specific segment, the TSS is defined by selector value stored in the system segment register.

Bit	Name	Attribute	Description
16-0	TSSS	R/W	Selector of TSS descriptor. The TSSR holds the 16-bit selector for the TSS descriptor.

11.2 I/O Mapped Registers

11.2.1 PCI Configuration Registers

I/O Port: CF8h ─ Accessed as a Dword

Register Name: PCI Configuration Address Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CE	Rsvd							BN								DN					FN			RN						Rsvd	

Configuration Address Register is a 32-bit register accessed only when referenced as a Dword. A byte or word reference will pass through the Configuration Address Register onto the PCI bus as an I/O cycle.

Bit	Name	Attribute	Description
31	CE	R/W	Configuration Enable. When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30-24	Rsvd	RO	Reserved.
23-16	BN	R/W	Bus Number. When the bus number is programmed to 00h, the target of the configuration cycle is either the North-Bridge or the PCI Device that is connected to the North-Bridge. If the bus number is programmed to 00h and the North-Bridge is not the target, a Type 0 configuration cycle is generated on PCI Bus. IF the bus number is non-zero, a Type 1 configuration cycle is generated on PCI bus with the bus number mapped to AD[23:16] during the address phase.
15-11	DN	R/W	Device Number. This field selects one agent on the PCI bus. During a Type 1 configuration cycle, this field is mapped to AD[15:11]. During a Type 0 configuration cycle, this field is decoded and one of AD[31:11] is driven to 1. The R8870 is always Device number 0.
10-8	FN	R/W	Function Number. This field allows the configuration registers of a particular function in a multi-function device to be accessed. The R3210 North Bridge only responds to configuration cycle with a function number of 000b.
7-2	RN	R/W	Register Number. This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register.
1-0	Rsvd	RO	Reserved.

I/O Port: CFCh – Accessed as a Dword
Register Name: PCI Configuration Data Register
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDR																															

Configuration Data Register is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by Configuration Data Register is determined by the contents of Configuration Address Register.

Bit	Name	Attribute	Description
31-0	CDR	R/W	If bit 31 of PCI Configuration Address Register is 1, any I/O reference that falls in the PCI Configuration Data Register space is mapped to configuration space using the contents of PCI Configuration Address Register.

11.2.2 Slave DMA Control Registers

I/O Port: 00h
Register Name: Slave DMA Channel 0 Base/Current Address Register
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

Bit	Name	Attribute	Description
7-0	BA/CA	R/W	Read: Current Address Register Read the 16-bit Current Address Register for DMA channel 0. The first 8-bit read will return the low portion of the word, and the second read will return the upper portion of the word. The current Address Register holds the current memory address used in a DMA transfer. It is automatically incremented or decremented after each DMA memory transfer. Write: Base and Current Address Register Two sequential 8-bit I/O writes load a 16-bit value into this register. The first 8-bit write loads the low portion of the word, and the second 8-bit write loads the high portion of the word. The Base Address Register is Write-Only. The Base Address Register is used to hold the original value of the Current Address Register, and is not incremented or decremented during the DMA transfer.

I/O Port: 01h
Register Name: Slave DMA Channel 0 Base/Current Count
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

Bit	Name	Attribute	Description
7-0	BC/CC	R/W	Read: Current Count Register Read the 16-bit Current Count Register for DMA channel 0. The first 8-bit read will return the low portion of the word, and the second read will return the upper portion of the word. The Current Count Register holds 1 plus the remaining number of transfers to occur. A value of 100h indicates 101h transfers remain. This register is decremented after each transfer. When the register rolls from 0 to FFFFh, the transfer is complete. Write: Base and Current Count Register Two sequential 8-bit I/O writes load a 16-bit value into this register. The first 8-bit write loads the low portion of the word, and the second 8-bit write loads the high portion of the word. The Base Count Register is Write-Only. The Base Count Register is used to hold the original value of the Current Count Register.

I/O Port: 02h
Register Name: Slave DMA Channel 1 Base/Current Address Register
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

The definitions of bit[7:0] for Slave DMA Channel 1 Base/Current Address are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Address Register at I/O address 00h.

I/O Port: 03h
Register Name: Slave DMA Channel 1 Base/Current Count Register
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

The definitions of bit[7:0] for Slave DMA Channel 1 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 01h.

I/O Port: 04h
Register Name: Slave DMA Channel 2 Base/Current Address Register
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

The definitions of bit[7:0] for Slave DMA Channel 2 Base/Current Address are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Address Register at I/O address 00h.

I/O Port: 05h
Register Name: Slave DMA Channel 2 Base/Current Count Register
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

The definitions of bit[7:0] for Slave DMA Channel 2 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 01h.

I/O Port: 06h
Register Name: Slave DMA Channel 3 Base/Current Address Register
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

The definitions of bit[7:0] for Slave DMA Channel 3 Base/Current Address are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Address Register at I/O address 00h.

I/O Port: 07h
Register Name: Slave DMA Channel 3 Base/Current Count Register
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

The definitions of bit[7:0] for Slave DMA Channel 3 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 01h.

I/O Port: 08h
Register Name: Slave DMA Status/Command Register
Reset Value: 00000010b/00x0x0x0

READ: Status Register

The Status register is available to be read out of the 82C37A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bit 0-3 are set every time a TC is reached by that channel or an external EOP is applied. These bits are cleared upon RESET, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, the Status register can be polled by software to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bit 4-7 are updated while the clock is high, and latched on the falling edge. Status Bit 4-7 are cleared upon RESET or Master Clear.

7	6	5	4	3	2	1	0
C3REQ	C2REQ	C1REQ	C0REQ	C3TC	C2TC	C1TC	C0TC

Bit	Name	Attribute	Description
7	C3REQ	R	= 1 DMA Channel 0 request
6	C2REQ	R	= 1 DMA Channel 0 request
5	C1REQ	R	= 1 DMA Channel 0 request
4	C0REQ	R	= 1 DMA Channel 0 request
3	C3TC	R	= 1 DMA Channel 3 has reached terminal count
2	C2TC	R	= 1 DMA Channel 2 has reached terminal count
1	C1TC	R	= 1 DMA Channel 1 has reached terminal count
0	C0TC	R	= 1 DMA Channel 0 has reached terminal count

Write: Command Register

This 8-bit register controls the operation of the DMA. The register is cleared by a hardware reset or a Master Disable instruction (port 0Dh). The command value used by PCs is 0. Normally all bits are left at 0, except bit 2 is typically set to 1 to disable the controller while writing to DMA registers. This register is a write-only.

7	6	5	4	3	2	1	0
ACKSL	REQSL	WS	PRI	TIM	CTL	AH	MMT

Bit	Name	Attribute	Description
7	ACKSL	W	= 1: DACK sense active high = 0: DACK sense active low
6	REQSL	W	= 1: DREQ sense active low = 0: DREQ sense active high
5	WS	W	= 1: Extended write selection = 0: Late write selection = X: if bit-3 = 0
4	PRI	W	= 1: Rotating priority = 0: Fixed priority
3	TIM	W	= 1: Compressed timing = 0: Normal timing = X: if bit-1 = 0
2	CTL	W	= 1: Control disable = 0: Control enable
1	AH	W	= 1: Channel 0 address hold enable = 0: Channel 0 address hold disable = X: if bit-0 = 0
0	MMT	W	= 1: Memory-to-memory transfers enable = 0: Memory-to-memory transfers disable

I/O Port: 09h
Register Name: Slave DMA Request Register
Reset Value: --

7	6	5	4	3	2	1	0
Reserved					SR	CS	

In addition to initiating a request for DMA service by asserting a hardware request line, software can also initiate a DMA request. The Request Register is used to both set and clear any channel's request bit. The DMA controller does need to be in Block mode to use this function, as set in the Mode Register (port 0Bh). This register is write-only.

Bit	Name	Attribute	Description
7-3	Rsvd	RO	Reserved
2	SR	W	= 1: Set request bit = 0: Clear request bit
1-0	CS	W	= 00: Channel 0 select = 01: Channel 1 select = 10: Channel 2 select = 11: Channel 3 select

I/O Port: 0Ah
Register Name: Slave DMA Mask Register
Reset Value: --

7	6	5	4	3	2	1	0
Rsvd					SM	CS	

The mask register is used to disable or enable individual incoming requests. Setting a mask bit on disables the selected channel. Hardware reset disables all channels by setting all mask bits.

Bit	Name	Attribute	Description
7-3	Rsvd	RO	Reserved
2	SM	W	= 1: Set mask bit = 0: Clear mask bit
1-0	CS	W	= 00: Channel 0 select = 01: Channel 1 select = 10: Channel 2 select = 11: Channel 3 select

I/O Port: 0Bh
Register Name: Slave DMA Mode Register
Reset Value: --

7	6	5	4	3	2	1	0
MT		AD/AI	ATI	TT		CS	

The Mode Register indicates the mode of operation for each of the four DMA channel 0 to 3. Each channel has a separate 6-bit mode register and each is loaded through the Mode Register port.

Bit	Name	Attribute	Description
7-6	MT	W	Mode Type Selection. = 00: Demand mode = 01: Single mode = 10: Block mode = 11: Cascade mode
5	AD/AI	W	= 1: Address decrement select = 0: Address increment select
4	ATI	W	= 1: Autoinitialization enable = 0: Autoinitialization disable
3-2	TT	W	Transfer Type. = 00: Verify operation = 01: Write operation = 10: Read operation = 11: not valid = xx: if they are in cascade mode (bit 6 & 7)
1-0	CS	W	Channel Selection. = 00: Channel 0 select = 01: Channel 1 select = 10: Channel 2 select = 11: Channel 3 select

I/O Port: 0Ch
Register Name: Slave DMA Set/Clear First/Last Clear F/F Register
Reset Value: --

7	6	5	4	3	2	1	0
CFF							

Bit	Name	Attribute	Description
7-0	CFF	W	Any value to this port causes the internal First/Last flip-flop to be cleared in DMA controller 1. This is done before any 8-bit reads or writes to 16-bit registers that require two successive 8-bit port accesses to complete the word transfer. After the flip-flop is cleared, a 16-bit DMA register is accessed by reading or writing the low byte followed by the high byte. The flip-flop can only be cleared, and is not readable.

I/O Port: 0Dh
Register Name: Slave DMA Temporary/Master Disable Register
Reset Value: --

7	6	5	4	3	2	1	0
TP/MD							

Bit	Name	Attribute	Description
7-0	TP/MD	R/W	Read: Temporary Register. The Temporary Register holds data during memory-to-memory data transfers. After the transfer is complete, the Temporary Register holds the last data transfer. The Temporary Register can be read when the DMA controller is not performing a DMA transfer. The register is cleared by a reset. Write: Master Disable Register. Writing any value to this port resets the DMA controller. This command has the same action as a hardware reset. The mask register is set (channel 0 to 3 are disabled). The Command, Status, Request, Temporary, and the Byte flip-flop are all cleared.

I/O Port: 0Eh
Register Name: Slave DMA Clear Mask Register
Reset Value: --

7	6	5	4	3	2	1	0
CM							

Bit	Name	Attribute	Description
7-0	CM	W	Clear Mask Register. Writing any value to this port clears the mask register. Clearing the Mask Register will enable all four channels to accept DMA requests. This register is write-only.

I/O Port: 0Fh
Register Name: Slave DMA Write Mask Register
Reset Value: xxxx_0000b

7	6	5	4	3	2	1	0
Rsvd				C3SM	C2SM	C1SM	C0SM

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved
3	C3SM	W	= 1: Channel 3 set mask bit = 0: Channel 3 clear mask bit
2	C2SM	W	= 1: Channel 2 set mask bit = 0: Channel 2 clear mask bit
1	C1SM	W	= 1: Channel 1 set mask bit = 0: Channel 1 clear mask bit
0	C0SM	W	= 1: Channel 0 set mask bit = 0: Channel 0 clear mask bit

11.2.3 DMA Pager Registers

I/O Port: 81h
Register Name: DMA Page Register – DMA Channel 2
Reset Value: --

7	6	5	4	3	2	1	0
DP2							

Bit	Name	Attribute	Description
7-0	DP2	W/R	This register holds the address bits A[23:16] to use for DMA transfers to memory for channel 2. The lower 16 bits of address are generated by the DMA conrtoller. This allows DMA transfers in the first 16MB of memory.

I/O Port: 82h
Register Name: DMA Page Register – DMA Channel 3
Reset Value: --

7	6	5	4	3	2	1	0
DP3							

Bit	Name	Attribute	Description
7-0	DP3	W/R	This register holds the address bits A[23:16] to use for DMA transfers to memory for channel 3. The lower 16 bits of address are generated by the DMA controller. This allows DMA transfers in the first 16MB of memory.

I/O Port: 83h
Register Name: DMA Page Register – DMA Channel 1
Reset Value: --

7	6	5	4	3	2	1	0
DP1							

Bit	Name	Attribute	Description
7-0	DP1	W/R	This register holds the address bits A[23:16] to use for DMA transfers to memory for channel 1. The lower 16 bits of address are generated by the DMA controller. This allows DMA transfers in the first 16MB of memory.

I/O Port: 87h
Register Name: DMA Page Register – DMA Channel 0
Reset Value: --

7	6	5	4	3	2	1	0
DP0							

Bit	Name	Attribute	Description
7-0	DP0	W/R	This register holds the address bits A[23:16] to use for DMA transfers to memory for channel 0. The lower 16 bits of address are generated by the DMA controller. This allows DMA transfers in the first 16MB of memory.

I/O Port: 89h
Register Name: DMA Page Register – DMA Channel 6
Reset Value: --

7	6	5	4	3	2	1	0
DP6							

Bit	Name	Attribute	Description
7-0	DP6	W/R	This register holds the address bits A[23:17] to use for DMA transfers to memory for channel 6. The lower 16 bits of address A[16:1] are generated by the DMA conttoller. A[0] is forced to 0. This allows DMA transfers in the first 16MB of memory.

I/O Port: 8Ah
Register Name: DMA Page Register – DMA Channel 7
Reset Value: --

7	6	5	4	3	2	1	0
DP7							

Bit	Name	Attribute	Description
7-0	DP7	W/R	This register holds the address bits A[23:17] to use for DMA transfers to memory for channel 7. The lower 16 bits of address A[16:1] are generated by the DMA controller, A[0] is forced to 0. This allows DMA transfers in the first 16MB of memory.

I/O Port: 8Bh
Register Name: DMA Page Register – DMA Channel 5
Reset Value: --

7	6	5	4	3	2	1	0
DP5							

Bit	Name	Attribute	Description
7-0	DP5	W/R	This register holds the address bits A[23:17] to use for DMA transfers to memory for channel 5. The lower 16 bits of address A[16:1] are generated by the DMA controller, A[0] is forced to 0. This allows DMA transfers in the first 16MB of memory.

11.2.4 Master DMA Control Registers

I/O Port: C0h
Register Name: Master DMA Base/Current Address Register ─ DMA Channel 4
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

Bit	Name	Attribute	Description
7-0	BA/CA	R/W	DMA Channel 4 is used for a cascade function from slave DMA. Channel 4 is unavailable for other uses.

I/O Port: C2h
Register Name: Master DMA Base/Current Count Register ─ DMA Channel 4
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

Bit	Name	Attribute	Description
7-0	BC/CC	R/W	DMA Channel 4 is used for a cascade function from slave DMA. Channel 4 is unavailable for other uses.

I/O Port: C4h
Register Name: Master DMA Base/Current Address Register ─ DMA Channel 5
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

On AT and EISA systems, DMA channel 5 is an unassigned channel, used for high-speed transfers between memory and the I/O bus. On PS/2, channel 5 is used for hard disk DMA operations.

The definitions of bit[7:0] for Slave DMA Channel 1 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 00h.

I/O Port: C6h
Register Name: Master DMA Base/Current Count Register – DMA Channel 5
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

On AT and EISA systems, DMA channel 5 is an unassigned channel, used for high-speed transfers between memory and the I/O bus. On PS/2, channel 5 is used for hard disk DMA operations.

The definitions of bit[7:0] for Slave DMA Channel 1 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 01h.

I/O Port: C8h
Register Name: Master DMA Base/Current Address Register – DMA Channel 6
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

DMA Channel 6 is an unassigned channel, used for high-speed transfers between memory and the I/O bus.

The definitions of bit[7:0] for Slave DMA Channel 6 Base/Current Address are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Address Register at I/O address 00h.

I/O Port: CAh
Register Name: Master DMA Base/Current Count Register – DMA Channel 6
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

DMA Channel 6 is an unassigned channel, used for high-speed transfers between memory and the I/O bus.

The definitions of bit[7:0] for Slave DMA Channel 2 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 01h.

I/O Port: CCh
Register Name: Master DMA Base/Current Address Register ─ DMA Channel 7
Reset Value: --

7	6	5	4	3	2	1	0
BA/CA							

DMA Channel 7 is an unassigned channel, used for high-speed transfers between memory and the I/O bus.

The definitions of bit[7:0] for Slave DMA Channel 3 Base/Current Address are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Address Register at I/O address 00h.

I/O Port: CEh
Register Name: Master DMA Base/Current Count Register ─ DMA Channel 7
Reset Value: --

7	6	5	4	3	2	1	0
BC/CC							

DMA Channel 7 is an unassigned channel, used for high-speed transfers between memory and the I/O bus.

The definitions of bit[7:0] for Slave DMA Channel 3 Base/Current Count are the same as those of bit[7:0] for Slave DMA Channel 0 Base/Current Count Register at I/O address 01h.

I/O Port: D0h
Register Name: Slave DMA Status/Command Register
Reset Value: 00000010b/00x0x0x0

READ: Status Register

7	6	5	4	3	2	1	0
C7REQ	C6REQ	C5REQ	C4REQ	C7TC	C6TC	C5TC	C4TC

The DMA Status Register holds flag (bit 0-3) indicating when each channel has reached the Terminal Count (transfer completed). When this register is read, these lower four bits are cleared. The status register also contains flags for pending DMA requests on each of the four channels. DMA requests occur by associating the desired DMA channel request line.

Bit	Name	Attribute	Description
7	C7REQ	R	= 1: DMA Channel 7 request
6	C6REQ	R	= 1: DMA Channel 6 request
5	C5REQ	R	= 1: DMA Channel 5 request

4	C4REQ	R	DMA Channel 4 used for cascade
3	C7TC	R	= 1: DMA Channel 7 has reached terminal count
2	C6TC	R	= 1: DMA Channel 6 has reached terminal count
1	C5TC	R	= 1: DMA Channel 5 has reached terminal count
0	C4TC	R	DMA Channel 4 used for cascade

Write: Command Register

This 8-bit register controls the operation of the DMA. The register is cleared by a hardware reset or a Master Disable instruction (port DAh). The command value used by PCs is 0. Normally all bits are left at 0, except bit 2 is typically set to 1 to disable the controller while writing to DMA registers. This register is write-only.

7	6	5	4	3	2	1	0
ACKSL	REQSL	WS	PRI	TIM	CTL	AH	MMT

Bit	Name	Attribute	Description
7	ACKSL	W	= 1: DACK sense active high = 0: DACK sense active low
6	REQSL	W	= 1: DREQ sense active low = 0: DREQ sense active high
5	WS	W	= 1: Extended write selection = 0: Late write selection = X: if bit 3 = 0
4	PRI	W	= 1: Rotating priority = 0: Fixed priority
3	TIM	W	= 1: Compressed timing = 0: Normal timing = X: if bit 1 = 0
2	CTL	W	= 1: Control disable = 0: Control enable
1	AH	W	= 1: Channel 4 address hold enable = 0: Channel 4 addrese hold disable = X: if bit 0 = 0
0	MMT	W	= 1: Memory-to-memory transfers enable = 0: Memory-to-memory transfers disable

I/O Port: D2h
Register Name: Master DMA Command/Request Register
Reset Value: --

7	6	5	4	3	2	1	0
Rsvd					SR	CS	

In addition to initiating a request for DMA service by asserting a hardware request line, software can also initiate a DMA request. The Request Register is used to both set and clear any channel's soft request bit. The DMA controller does need to be in Block

mode to use this function, as set in the Mode Register (port D6h).When reading the Request register, bits4-7 will always read as ones, and bits 0-3 will display the request bits of channels 4-7 respectively

write command

Bit	Name	Attribute	Description
7-3	Rsvd	RO	Reserved.
2	SR	W	= 1: Set request bit = 0: Clear request bit
1-0	CS	W	= 00: Channel 4 select = 01: Channel 5 select = 10: Channel 6 select = 11: Channel 7 select

read request

Bit	Name	Attribute	Description
7-4	Rsvd	RO	4'b1111
3	SDRQ7	RO	soft request register , channel 7
2	SDRQ6	RO	soft request register , channel 6
1	SDRQ5	RO	soft request register , channel 5
0	SDRQ4	RO	soft request register , channel 4

I/O Port: D4h
Register Name: Master DMA Mask Register
Reset Value: --

7	6	5	4	3	2	1	0
Rsvd					SM	CS	

The mask register is used to disable or enable individual incoming requests. Setting a mask bit on disables the selected channel. Hardware reset disables all channels by setting all mask bits.

Bit	Name	Attribute	Description
7-3	Rsvd	RO	Reserved
2	SM	W	= 1: Set mask bit = 0: Clear mask bit
1-0	CS	W	= 00: Channel 4 select = 01: Channel 5 select = 10: Channel 6 select = 11: Channel 7 select

I/O Port: D6h
Register Name: Master DMA Mode Register
Reset Value: --

7	6	5	4	3	2	1	0
MT		AD/AI	ATI	TT		CS	

The Mode Register indicates the mode of operation for each of the four DMA channels 4 to 7. Each channel has a separate 6-bit mode register and each is loaded through the Mode Register port.

Bit	Name	Attribute	Description
7-6	MT	W	Mode Type Selection. = 00: Demand mode = 01: Single mode = 10: Block mode = 11: Cascade mode
5	AD/AI	W	= 1: Address decrement select = 0: Address increment select
4	ATI	W	= 1: Autoinitialization enable = 0: Autoinitialization disable
3-2	TT	W	Transfer Type. = 00: Verify operation = 01: Write operation = 10: Read operation = 11: not valid = xx: if they are in cascade mode (bits 6 & 7)
1-0	CS	W	Channel Selection. = 00: Channel 4 select = 01: Channel 5 select = 10: Channel 6 select = 11: Channel 7 select

I/O Port: D8h
Register Name: Master DMA Set/Clear First/Last Clear F/F Register
Reset Value: --

7	6	5	4	3	2	1	0
CFF							

Bit	Name	Attribute	Description
7-0	CFF	W	Any value to this port causes the internal First/Last flip-flop to be cleared in DMA controller 1. This is done before any 8-bit reads or writes to 16-bit registers that require two successive 8-bit port accesses to complete the word transfer. After the flip-flop is cleared, a 16-bit DMA register is accessed by reading or writing the low byte followed by the high byte. The flip-flop can only be cleared, and is not readable.

I/O Port: DAh
Register Name: Master DMA Temporary/Master Disable Register
Reset Value: --

7	6	5	4	3	2	1	0
TP/MD							

Bit	Name	Attribute	Description
7-0	TP/MD	R/W	Read: Temporary Register. The Temporary Register holds data during memory-to-memory data transfers. After the transfer is complete, the Temporary Register holds the last data transfer. The Temporary Register can be read when the DMA controller is not performing a DMA transfer. The register is cleared by a reset. Write: Master Disable Register. Writing any value to this port resets master DMA control. This command has the same action as a hardware reset. The mask register is set (channel 4 to 7 disabled). The Command, Status, Request, Temporary, and the Byte flip-flop are all cleared.

I/O Port: DCh
Register Name: Master DMA Clear Mask Register
Reset Value: --

7	6	5	4	3	2	1	0
CM							

Bit	Name	Attribute	Description
7-0	CM	W	Clear Mask Register. Writing any value to this port clears the mask register. Clearing the Mask Register will enable channels 5, 6, and 7 to accept DMA requests. This register is write-only.

I/O Port: DEh
Register Name: Master DMA Write Mask Register
Reset Value: xxxx_0000b

7	6	5	4	3	2	1	0
Rsvd				C7SM	C6SM	C5SM	C4SM

The mask register is used to disable or enable individual incoming requests. Setting a mask bit on disables the selected channel. A hardware reset disables all channels by setting all mask bits.

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved
3	C7SM	W	= 1: Channel 7 sets mask bit = 0: Channel 7 clears mask bit
2	C6SM	W	= 1: Channel 6 sets mask bit = 0: Channel 6 clears mask bit
1	C5SM	W	= 1: Channel 5 sets mask bit = 0: Channel 5 clears mask bit
0	C4SM	W	= 1: Channel 4 sets mask bit = 0: Channel 4 clears mask bit

11.2.5 DMA High Page Registers

I/O Port: 481h
Register Name: DMA High Page Register – DMA Channel 2
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP2							

Bit	Name	Attribute	Description
7-0	DHP2	W/R	This register holds the address bits A[31:24] to use for DMA transfers for channel 2. Always write this register after the base and low page registers are written. A write to this channel's base address register or a write to the low page register at port 81h automatically clears this register. This ensures compatibility with DMA on AT system.

I/O Port: 482h
Register Name: DMA High Page Register – DMA Channel 3
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP3							

Bit	Name	Attribute	Description
7-0	DHP3	W/R	This register holds the upper 8 bits of the 32-bit address for channel 3. See port 481h for details.

I/O Port: 483h
Register Name: DMA High Page Register – DMA Channel 1
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP1							

Bit	Name	Attribute	Description
7-0	DHP1	W/R	This register holds the upper 8 bits of the 32-bit address for channel 1. See port 481h for details.

I/O Port: 487h
Register Name: DMA High Page Register – DMA Channel 0
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP0							

Bit	Name	Attribute	Description
7-0	DHP0	W/R	This register holds the upper 8 bits of the 32-bit address for channel 0. See port 481h for details.

I/O Port: 489h
Register Name: DMA High Page Register – DMA Channel 6
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP6							

Bit	Name	Attribute	Description
7-0	DHP6	W/R	This register holds the upper 8 bits of the 32-bit address for channel 6. See port 481h for details.

I/O Port: 48Ah
Register Name: DMA High Page Register – DMA Channel 7
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP7							

Bit	Name	Attribute	Description
7-0	DHP7	W/R	This register holds the upper 8 bits of the 32-bit address for channel 7. See port 481h for details.

I/O Port: 48Bh
Register Name: DMA High Page Register – DMA Channel 5
Reset Value: 00h

7	6	5	4	3	2	1	0
DHP5							

Bit	Name	Attribute	Description
7-0	DHP5	W/R	This register holds the upper 8 bits of the 32-bit address for channel 5. See port 481h for details.

11.2.6 Timer/Counter Registers

Note: The following clock is 14.318 MHz /12 (external) or 12.5 MHz /12 (internal).

I/O Port: 40h
Register Name: Timer/Counter 0 Count Register
Reset Value: --

7	6	5	4	3	2	1	0
T0							

Bit	Name	Attribute	Description
7-0	T0	R/W	Timer 0 is used for system clocking. It is normally programmed for mode 3, periodic square wave operation. The Count is loaded with 0 to generate a pulse 18.2 times per second.

I/O Port: 41h
Register Name: Timer/Counter 1 Count Register
Reset Value: --

7	6	5	4	3	2	1	0
T1							

Bit	Name	Attribute	Description
7-0	T1	R/W	Timer 1 is used for DRAM refresh. It is normally programmed for mode 2, rate generator operation. The count is loaded with 12h to generate a pulse every 15 us.

I/O Port: 42h
Register Name: Timer/Counter 2 Count Register
Reset Value: --

7	6	5	4	3	2	1	0
T2							

Bit	Name	Attribute	Description
7-0	T2	R/W	Timer 2 is used for speaker operations and general purpose.

I/O Port: 43h
Register Name: Timer/Counter Control Register
Reset Value: --

7	6	5	4	3	2	1	0

CMD	MS	CM

All the three timers are controlled by the modes set through this register.

Bit	Name	Attribute	Description
7-4	CMD	W	Command. 0h: Counter Latch Timer 0 1h: Timer 0 LSB Mode 2h: Timer 0 MSB Mode 3h: Timer 0 16-bit Mode 4h: Counter Latch Timer 1 5h: Timer 1 LSB Mode 6h: Timer 1 MSB Mode 7h: Timer 1 16-bit Mode 8h: Counter Latch Timer 2 9h: Timer 2 LSB Mode Ah: Timer 2 MSB Mode Bh: Timer 2 16-bit Mode Dh: General Counter Latch Eh: Latch Status of Timers
3-1	MS	W	000b: Mode 0 001b: Mode 1 010b: Mode 2 011b: Mode 3 100b: Mode 4 101b: Mode 5 110b: Mode 2 111b: Mode 3
0	CM	W	0b: Binary Counter mode (16-bit) 1b: BCD Counter mode (4 Binary Coded Decimal digits)

11.2.7 Master Interrupt Control Registers

I/O Port: 20h

Register Name: Master Interrupt Request/Interrupt Service/Interrupt Command Register

Reset Value: --

7	6	5	4	3	2	1	0
IRR/ISR/ICR							

Bit	Name	Attribute	Description
7-0	IRR/ISR/ICR	R/W	**Read:** Interrupt Request/Interrupt Service Register. This function reads the contents of the Interrupt Request Register (IRR) or the Interrupt Service Register (ISR). You specify which register to read by sending a command to port 20h. A command value of 0Ah selects IRR, and value 0Bh selects ISR. Once a command is sent, multiple reads can be made to get the contents of the same register. It is not necessary to resend the register selection command. **Write:** Interrupt Command Register. This controls initialization and operation of the interrupt controller for interrupt request line 0 to 7.

I/O Port: 21h

Register Name: Master Interrupt Mask Register
Reset Value: --

7	6	5	4	3	2	1	0
I7M	I6M	I5M	I4M	I3M	I2M	I1M	I0M

The interrupt mask register indicates which interrupt requests are allowed (value 0) and disabled (value 1).

Bit	Name	Attribute	Description
7	I7M	R/W	= 0: IRQ 7 Enabled = 1: IRQ 7 Disabled
6	I6M	R/W	= 0: IRQ 6 Enabled = 1: IRQ 6 Disabled
5	I5M	R/W	= 0: IRQ 5 Enabled = 1: IRQ 5 Disabled
4	I4M	R/W	= 0: IRQ 4 Enabled = 1: IRQ 4 Disabled
3	I3M	R/W	= 0: IRQ 3 Enabled = 1: IRQ 3 Disabled
2	I2M	R/W	= 0: IRQ 2 Enabled = 1: IRQ 2 Disabled
1	I1M	R/W	= 0: IRQ 1 Enabled = 1: IRQ 1 Disabled
0	I0M	R/W	= 0: IRQ 0 Enabled = 1: IRQ 0 Disabled

11.2.8 Slave Interrupt Control Registers

I/O Port: A0h
Register Name: Slave Interrupt Request/Interrupt Service/Interrupt Command Register
Reset Value: --

7	6	5	4	3	2	1	0
IRR/ISR/ICR							

Bit	Name	Attribute	Description
7-0	IRR/ISR/ ICR	R/W	**Read:** Interrupt Request/Interrupt Service Register. This function reads the contents of the Interrupt Request Register (IRR) or the Interrupt Service Register (ISR). You specify which register to read by sending a command to port A0h. A command value of 0Ah selects IRR, and value 0Bh selects ISR. Once a command is sent, multiple reads can be made to get the contents of the same register. It is not necessary to resend the register selection command. **Write:** Interrupt Command Register. This controls initialization and operation of the interrupt controller for interrupt request line 8 to 15.

I/O Port: A1h
Register Name: Slave Interrupt Mask Register
Reset Value: --

7	6	5	4	3	2	1	0
I15M	I14M	I13M	I12M	I11M	I10M	I9M	I8M

The interrupt mask register indicates which interrupt requests are allowed (value 0) and which are disabled (value 1).

Bit	Name	Attribute	Description
7	I15M	R/W	= 0: IRQ 15 Enabled = 1: IRQ 15 Disabled
6	I14M	R/W	= 0: IRQ 14 Enabled = 1: IRQ 14 Disabled
5	I13M	R/W	= 0: IRQ 13 Enabled = 1: IRQ 13 Disabled
4	I12M	R/W	= 0: IRQ 12 Enabled = 1: IRQ 12 Disabled
3	I11M	R/W	= 0: IRQ 11 Enabled = 1: IRQ 11 Disabled
2	I10M	R/W	= 0: IRQ 10 Enabled = 1: IRQ 10 Disabled
1	I9M	R/W	= 0: IRQ 9 Enabled = 1: IRQ 9 Disabled
0	I8M	R/W	= 0: IRQ 8 Enabled = 1: IRQ 8 Disabled

11.2.9 Interrupt Edge/Level Control Registers

I/O Port: 4D0h
Register Name: Master Interrupt Edge/Level Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
IR7TM	IR6TM	IR5TM	IR4TM	IR3TM	IR2TM	IR1TM	IR0TM

This register controls the triggering type for each IRQ line. Clear the bit to program edge sensitive. Set the bit to program level sensitive mode. Before writing this register, read the contents first. Do not change the state of IRQ 0, 1 and 2 bits, as these are set by the motherboard manufacturer's BIOS to reflect the specific board design.

Bit	Name	Attribute	Description
7	IR7TM	R/W	IRQ7 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
6	IR6TM	R/W	IRQ6 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
5	IR5TM	R/W	IRQ5 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
4	IR4TM	R/W	IRQ4 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
3	IR3TM	R/W	IRQ3 Edge/Level Triggered Mode

			0: Edge Triggered Mode 1: Level Triggered Mode
2	IR2TM	RO	IRQ2 Triggered Mode (do not change it)
1	IR1TM	RO	IRQ1 Triggered Mode (do not change it)
0	IR0TM	RO	IRQ0 Triggered Mode (do not change it)

I/O Port: 4D1h
Register Name: Slave Interrupt Edge/Level Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
IR15TM	IR14TM	IR13TM	IR12TM	IR11TM	IR10TM	IR9TM	IR8TM

This register controls the triggering type for each IRQ line. Clear the bit to program edge sensitive. Set the bit to program level sensitive mode. Before writing this register, read the contents first. Do not change the state of IRQ 8 and IRQ 13, as these are set by the motherboard manufacturer's BIOS to reflect the specific board design.

Bit	Name	Attribute	Description
7	IR15TM	R/W	IRQ15 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
6	IR14TM	R/W	IRQ14 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
5	IR13TM	RO	IRQ13 Triggered Mode (do not change)
4	IR12TM	R/W	IRQ12 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
3	IR11TM	R/W	IRQ11 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
2	IR10TM	R/W	IRQ10 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
1	IR9TM	R/W	IRQ9 Edge/Level Triggered Mode 0: Edge Triggered Mode 1: Level Triggered Mode
0	IR8TM	RO	IRQ8 Triggered Mode (do not change it)

11.2.10 Serial Port Registers

The system programmer may access any of the UART registers. These registers control UART operations including transmission and reception of data.

(**Base Address** Refers to the Register of index 57h-54h, IDSEL = AD18 of PCI Configuration Register)

I/O Port: Base Address + 0h
Register Name: Transmit/Receive Data Buffer (DLAB=0)
Reset Value: --

7	6	5	4	3	2	1	0
TD/RD							

An output to this register stores a byte into the UART's transmit holding buffer. An input gets a byte from the receive buffer of the UART. These are two separate registers within the UART. To access this register, the Divisor Latch Access Bit (DLAB) must be zero. DLAB is bit 7 in the line control register 3.

Bit	Name	Attribute	Description
7-0	TD/RD	R/W	**Read:** This register holds the received incoming data byte. **Write:** This register contains the data byte to be transmitted.

I/O Port: Base Address + 0h
Register Name: LSB of Baud Rate Generator Divisor Latches (DLAB=1)
Reset Value: 01h

7	6	5	4	3	2	1	0
LBR							

The UART contains a programmable baud generator that is capable of taking any clock input from DC to 24 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the baud generator is 16 X the baud [divisor # = (frequency input) / (baud rate X 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. The Table listed below provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 18.432 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

Bit	Name	Attribute	Description
7-0	LBR	R/W	This register contains the LSB (Least Significant Byte) of divisor latches.

TABLE Baud Rates, Divisors and Crystals

Baud Rate	1.8432 MHz Crystal	
	Decimal Divisor for 16 X Clock	Percent Error
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-

1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.68
115200	1	-

I/O Port: Base Address + 1h
Register Name: Interrupt Enable Register (DLAB=0)
Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved				MSI	RLSI	THREI	RDAI

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bit 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the settings of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit are listed as follows.

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved. Must be always '0'
3	MSI	R/W	Modem Status Interrupt 0: Disable 1: Enable
2	RLSI	R/W	Received Line Status Interrupt 0: Disable 1: Enable
1	THREI	R/W	Transmitter Holding Register Empty Interrupt 0: Disable 1: Enable
0	RDAI	R/W	Received Data Available Interrupt 0: Disable 1: Enable

I/O Port: Base Address + 1h
Register Name: MSB of Baud Rate Generator Divisor Latches (DLAB=1)
Reset Value: 00h

7	6	5	4	3	2	1	0
MBR							

Bit	Name	Attribute	Description
7-0	MBR	R/W	This register contains the MSB (Most Significant Byte) of divisor latches.

I/O Port: Base Address + 2h
Register Name: Interrupt Identification Register
Reset Value: 01h

7	6	5	4	3	2	1	0
FIFOE		Rsvd		FIFOM	PT		IP

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status, Received Data Ready, Transmitter Holding Register Empty, and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table II shows the contents of the IIR. Details on each bit are listed as follows:

Bit	Name	Attribute	Description
7-6	FIFOE	RO	These two bits are set to ‘1’ when the FIFO Control Register bit 0 = ‘1’.
5-4	Rsvd	RO	Reserved. Must be returned all ‘0’s.
3	FIFOM	RO	In non-FIFO Mode This bit is a ‘0’. In FIFO Mode This bit is set to ‘1’ along with bit 2 when a timeout interrupt is pending
2-1	PT	RO	Indicate the Highest Priority Interrupt Pending 00: Modem Status Interrupt (Lowest Priority) 01: Transmitter Holding Register Empty Interrupt 10: Received Data Ready Interrupt 11: Receiver Line Status Interrupt (Highest Priority)
0	IP	RO	Interrupt Pending 0: Interrupt Pending 1: No Interrupt Pending

TABLE Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Rest Control
0	0	0	1	-	None	None	-
0	1	1	0	Highest	received line status	overrun error, parity error, framing error or break Interrupt	reading the line status register
0	1	0	0	Second	received data available	received data available or trigger level reached	reading the receiver buffer register or the FIFO dropping below the trigger level
1	1	0	0	Second	character timeout Indication	no characters have been removed from or Input to the RCVR FIFO during the last 4 Characters times and there is at least 1 character in it during this time.	reading the receiver buffer register
0	0	1	0	Third	transmitter holding register empty	transmitter holding register empty	reading the IIR register (if the source of interrupt is available) or writing into the transmitter holding register
0	0	0	0	Fourth	MODEM Status	clear to send, data set ready , ring Indicator, or data carrier detect	reading the MODEM Status register

I/O Port: Base Address + 2h

Register Name: FIFO Control Register

Reset Value: 00h

7	6	5	4	3	2	1	0
TL			Rsvd		CTF	CRF	FE

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Bit	Name	Attribute	Description
7-6	TL	WO	These two bits are used to set the trigger level (bytes) for Receive FIFO interrupt 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
5-3	Rsvd	RO	Reserved.
2	CTF	WO	Writing a ‘1’ to this bit will clear all bytes in transmitted FIFO and reset its counter to 0. The shift register is not cleared
1	CRF	WO	Writing a ‘1’ to this bit will clear all bytes in received FIFO and reset its counter to 0. The shift register is not cleared
0	FE	WO	Setting this bit to a "1" enables both the transmitted and received FIFOs. Clearing this bit to a "0" disables both the transmitted and received FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data are automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

I/O Port: Base Address + 3h
Register Name: Line Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
DLAB	BC	SP	EOP	PE	NSB	SCN	

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table II shows the contents of the LCR. Details on each bit are listed as follows:

Bit	Name	Attribute	Description
7	DLAB	R/W	Divisor Latch Access Bit (DLAB). It must be set to '1' to access the divisor latch of the baud generator during a Read or Write operation. It must be set to a '0' to access the Receive Buffer, the Transmitter Holding Register or the interrupt Enable Register.
6	BC	R/W	Break Control Bit. It causes a break condition to be transmitted to the receiving UART. 0: Disable the break 1: Force the serial out (SOUT) to the Spacing ('0') State
5	SP	R/W	This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1s, the Parity bit is transmitted and checked as a '0'. If bits 3 and 5 are '1's and bit 4 is a '0', the Parity bit is transmitted and checked as a '1'. If bit 5 is a logic 0, Stick Parity is disabled.
4	EOP	R/W	Even/Odd parity bit selected when parity is enabled 0: Odd parity selected 1: Even parity selected
3	PE	R/W	Parity Enabled/Disabled. 0: Parity disabled 1: Parity enabled When this bit is set to a '1', a parity bit will be generated between the last data word and STOP bit when data is being transmitted, and check the parity bit when data is being received.
2	NSB	R/W	Stop bit. This bit specifies the number of Stop bits transmitted and received in each serial character. Set 0: One Stop bit is generated in the transmitted data. Set 1: One and a half stop bits are generated for a 5-bit word length characters. Two stop bits are generated for either 6-, 7-, or 8-bit word length characters. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1-0	SCN	R/W	These two bits specify the number of bits in each transmitted and received serial characters. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

I/O Port: Base Address + 4h
Register Name: Modem Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
Rsvd			LBF	INTE	Rsvd	RTS	DTR

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described as below.

Bit	Name	Attribute	Description
7-5	Rsvd	RO	Reserved. Must be all '0's
4	LBF	R/W	This bit provides the loop back feature for diagnostic testing of the Serial Port. When this bit is set to '1', the following occurs: 1) The Transmitter serial out (SOUT) is set to the Marking State ('1'). 2) The receiver Serial Input (SIN) is disconnected. 3) The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input. 4) All MODEM Control inputs (CTS_n, DSR_n, RI_n and DCD_n) are disconnected. 5) The four MODEM Control outputs (DTR_n, RTS_n, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (CTS_n, DSR_n, RI_n and DCD_n). 6) The Modem Control output pins are forced to be inactive high. 7) Data transmitted are immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
3	INTE	R/W	Interrupt Enable. This bit is used to enable a UART interrupt. When OUT2 is a '0', the serial port interrupt output is forced to the high impedance state - disabled. When OUT2 is a '1', the serial port interrupt output is enabled.
2	Rsvd	RO	Reserved.
1	RTS	R/W	This bit controls the Request To Send (RTS_n) output. When this bit is set to a '1', the RTS_n output is forced to a '0'. When this bit is a '0', the RTS_n output is forced to a '1'.
0	DTR	R/W	This bit controls the Data Terminal Ready (DTR_n) output. When this bit is set to a '1', the DTR_n output is forced to a '0'. When this bit is a '0', the DTR_n output is forced to a '1'.

I/O Port: Base Address + 5h
Register Name: Line Status Register
Reset Value: 60h

7	6	5	4	3	2	1	0
EB	TEMT	THRE	BI	FE	PE	OE	DR

This register provides status information to the CPU concerning the data transfer.

Bit	Name	Attribute	Description

7	EB	R/W	This bit is permanently set to a logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.
6	TEMT	R/W	Transmitter Empty (TEMT). This bit is set to a '1' whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to a '0' whenever either the THR or TSR contains a data character. This bit is a read only bit. In the FIFO mode, this bit is set whenever the THR and TSR are both empty,
5	THRE	R/W	Transmitter Holding Register Empty (THRE). This bit indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a '1' when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. This bit is reset to '0' whenever the CPU loads the Transmitter Holding Register. In the FIFO mode, this bit is set when the transmit FIFO is empty. It is cleared when at least 1 byte is written to the transmit FIFO. This bit is a read only bit.
4	BI	R/W	Break Interrupt (BI). This bit is set to a '1' whenever the received data input is held in the Spacing state ('0') for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO. Restarting after a break is received requires the serial data (RXD) to be '1' for at least 1/2 bit time.
3	FE	R/W	Framing Error (FE). This bit indicates that the received character does not have a valid stop bit. This bit is set to a '1' whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a '0' whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.
2	PE	R/W	Parity Error (PE). This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a '1' upon detection of a parity error and is reset to a '0' whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.
1	OE	R/W	Overrun Error (OE). This bit indicates that the data in the Receiver Buffer Register were not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register. The character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a '1' immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.
0	DR	R/W	Data Ready (DR). It is set to a '1' whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. This bit is reset to a '0' by reading all of the data in the Receiver Buffer Register or the FIFO.

I/O Port: Base Address + 6h
Register Name: Modem Status Register
Reset Value: x0h

7	6	5	4	3	2	1	0
DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to logic 1s whenever a control input from the MODEM changes state. They are reset to logic 0s whenever the CPU reads the MODEM Status Register. The contents of the MODEM Status Register are indicated in Table II and described as below.

Bit	Name	Attribute	Description
7	DCD	R/W	This bit is the complement of the Data Carrier Detect (DCD_n) input. If bit 4 of the MCR is set to '1', this bit is equivalent to OUT2 in the Modem Control Register.
6	RI	R/W	This bit is the complement of the Ring Indicator (RI_n) input. If bit 4 of the MCR is set to '1', this bit is equivalent to OUT1 in the Modem Control Register.
5	DSR	R/W	This bit is the complement of the Data Set Ready (DSR_n) input. If bit 4 of the MCR is set to '1', this bit is equivalent to DTR_n in the Modem Control Register.
4	CTS	R/W	This bit is the complement of the Clear To Send (CTS_n) input. If bit 4 of the MCR is set to '1', this bit is equivalent to RTS_n in the Modem Control Register.
3	DDCD	R/W	Delta Data Carrier Detect (DDCD). This bit is set to '1' whenever the DCD_n input to the chip has changed the state since the last time the MSR (Modem Status Register) was read. It is reset to a '0' whenever the MODEM Status Register is read.
2	TERI	R/W	Trailing Edge of Ring Indicator (TERI). This bit is set to '1' whenever the RI_n input has been changed from '0' to '1'. It is reset to '0' whenever the MODEM Status Register is read.
1	DDSR	R/W	Delta Data Set Ready (DDSR). This bit indicates that the DSR_n input to R3210 has changed the state since the last time the MSR (Modem Status Register) was read. This bit is set to '1'" whenever DSR_n input from the MODEM has changed the state. It is reset to '0' whenever the MODEM Status Register is read.
0	DCTS	R/W	Delta Clear To Send (DCTS). This bit indicates that the CTS_n input to the R3210 has changed the state since the last time the MSR (Modem Status Register) was read. This bit is set to '1'" whenever CTS_n input from the MODEM has changed the state. It is reset to '0' whenever the MODEM Status Register is read.

Note: *Whenever bit 0, 1, 2 or 3 is set to a logic "1", a MODEM Status Interrupt is generated.*

I/O Port: Base Address + 7h
Register Name: Scratchpad Register
Reset Value: --

7	6	5	4	3	2	1	0
SR							

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register used by the programmer to hold data temporarily.

Bit	Name	Attribute	Description
7-0	SR	R/W	This 8-bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

11.2.11 NMI Status and Control Register

I/O Port: 61h
Register Name: NMI Status and Control Register
Reset Value: --

7	6	5	4	3	2	1	0
SSS	ISS	T2S	RCT	IOE	PSE	SDE	T2E

Bit	Name	Attribute	Description
7	SSS	RO	SERR_n NMI Source Status. Bit 7 is set if a system board agent (PCI devices or main memory) detects a system board error and pulses the PCI SERR_n line. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 0 and then set it to '1'. When writing to port 061, bit 7 must be a 0.
6	ISS	RO	IOCHK_n NMI Source Status. Bit 6 is set if an expansion board asserts an IOCHK_n on the ISA Bus. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 0 and then set it to '1'. When writing to port 061, bit 6 must be a 0.
5	T2S	RO	Timer Counter 2 OUT Status. The Counter 2 OUT signal state is reflected in Bit 5. The value on this bit following a read is the current state of the Counter 2 OUT signal. Counter 2 must be programmed by following a CPURST for this bit to have a determinate value. When writing to port 061, bit 5 must be a 0.
4	RCT	RO	Refresh Cycle Toggle. The Refresh Cycle Toggle signal toggles from either 0 to 1 or 1 to 0 by following every refresh cycle. When writing to port 061, bit 5 must be a 0.
3	IOE	R/W	1 = Clear and Disable. 0 = Enable IOCHK_n NMIs.
2	PSE	R/W	PCI SERR_n Enable. 1 = Clear and Disable. 0 = Enable.
1	SDE	R/W	Speaker Data Enable. 0 = SPKR output is 0. 1 = the SPKR output is the Counter 2 OUT signal value.
0	T2E	R/W	Timer Counter 2 Enable. 0 = Disable; 1 = Enable.

11.2.12 CMOS Memory & RTC Register

I/O Port: 70h
Register Name: CMOS Memory Address Register
Reset Value: --

7	6	5	4	3	2	1	0
ND	CRA						

This port is shared with the real-time clock. Do not modify the contents of this register without considering the effects on the state of the other bits. Reads and writes to this register address flow through to the ISA Bus. Reads to register 70h will cause X-Bus reads, but no RTCCS_n or RTCALE will be generated. (The RTC has traditionally been write-only to port 70h.)

Bit	Name	Attribute	Description
7	ND	W	= 1: NMI disabled = 0: NMI enabled
6-0	CRA	W	CMOS RAM address for the next read or write

I/O Port: 71h
Register Name: CMOS Memory Data Register
Reset Value: --

7	6	5	4	3	2	1	0
CRD							

Bit	Name	Attribute	Description
7-0	CRD	W/R	RTC Data. Data written to standard RAM bank address selected via CMOS Memory Address Register (70h).

11.2.13 System Function Register

I/O Port: 92h
Register Name: System Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved						FGA	FSR

Bit	Name	Attribute	Description
7-2	Rsvd	RO	Reserved. Returns “0” when read.
1	FGA	R/W	Fast Gate A20. Set ‘1’ to this bit and ‘0’ to Configuration Register Index 41 bit 1 to Turn ON the Fast Gate A20.
0	FSR	R/W	Fast System Reset. Set ‘1’ to this bit and ‘0’ to Configuration Register Index 41 bit 1 to Reset System

11.3 PCI Configuration Space Registers

11.3.1 R3210 North Bridge Configuration Registers

Register Offset: 01h – 00h
Register Name: Vendor ID Register
Reset Value: 17F3h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VID															

Bit	Name	Attribute	Description
15-0	VID	RO	This register contains a 16-bit value assigned to RDC Semiconductor Co., Ltd.

Register Offset: 03h – 02h
Register Name: Device ID Register
Reset Value: 6020h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID															

Bit	Name	Attribute	Description
15-0	DID	RO	This register contains a 16-bit value assigned to the R3210 device.

Register Offset: 05h – 04h
Register Name: Command Register
Reset Value: 000Eh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											MWIC	SCOC	MDC	MAC	IOAC

Bit	Name	Attribute	Description
15-5	Rsvd	RO	Reserved.
4	MWIC	RO	Memory Write and Invalid Command.
3	SCOC	RO	Special Cycle operations control.
2	MDC	RO	PCI Bus Master Device Control. This bit always returns ‘1’
1	MAC	RW	Memory Space Accesses Control. It controls a device’s response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses.
0	IOAC	RO	I/O Space Accesses Control.

Register Offset: 07h – 06h
Register Name: Status Register
Reset Value: 0400h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	SS	RMAS	RTAS	STAS	DT		Reserved								

Bit	Name	Attribute	Description
15	DPE	RO	Detected Parity Error. This bit must be set whenever the device detects a parity error. This is a read-only bit and is cleared by writing '1' to it.
14	SS	RO	SERR_n status. This bit must be set whenever the device asserts SERR_n. This is a read-only bit and is cleared by writing '1' to it.
13	RMAS	RO	Receive Master Abort Status when the R3210 acts as a master. This bit is set to '1' when the R3210 generates a transaction (except for Special Cycle), and is terminated with master abort. This is a read-only bit and is cleared by writing '1' to it.

12	RTAS	RO	Receive Target Abort Status when the R3210 acts as a master. This bit is set to '1' when the R3210 encounters a target abort condition. This is a read-only bit and is cleared by writing a '1' to it.
11	STAS	RO	Signal Target Abort Status when the R3210 acts as a slave. The R3210 as a slave never generates a target abort. This bit is always 0.
10-9	DT	RO	DEVSEL_n Timing. Only support Medium decode “01” & Slow decode “10”.
8-0	Rsvd	RO	Reserved. These bits always return ’0’s.

Register Offset: 08h
Register Name: Revision ID Register
Reset Value: 01h

7	6	5	4	3	2	1	0
RID							

Bit	Name	Attribute	Description
7-0	RID	RO	Version number of the R3210.

Register Offset: 0Bh – 09h
Register Name: Class Code Register
Reset Value: 060000h

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC																							

Bit	Name	Attribute	Description
23-0	CC	RO	Class Code of the R3210.

Register Offset: 0Eh
Register Name: Header Type Register
Reset Value: 00h

7	6	5	4	3	2	1	0
00h							

Bit	Name	Attribute	Description
7-0	HT	RO	This register identifies the type of predefined header in the configuration space. Since the R3210 is a single function device (bit7=’0’) and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Offset: 2Dh – 2Ch

Register Name: Subsystem Vendor ID Register
Reset Value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVID															

Bit	Name	Attribute	Description
15-0	SVID	RO	This register contains the subsystem Vendor ID.

Register Offset: 2Fh – 2Eh
Register Name: Subsystem Device ID Register
Reset Value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDID															

Bit	Name	Attribute	Description
15-0	SDID	RO	This register contains the subsystem Device ID.

Register Offset: 53h – 50h
Register Name: NonCache Region Register #1 for L1
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address																					En	Reserved								Size	

Bit	Name	Attribute	Description
31-11	BA	R/W	Base Address for the user-defined NonCache Region
10	REn	R/W	Region Enabled for the NonCache Region
9-3	Rsvd	R/W	Reserved
2-0	RSz	R/W	Size of the NonCache Region Bit 2 Bit 1 Bit 0 Size 0 0 0 2K Bytes 0 0 1 4K Bytes 0 1 0 8K Bytes 0 1 1 16K Bytes 1 0 0 32K Bytes 1 0 1 64K Bytes 1 1 0 128K Bytes 1 1 1 256K Bytes

Register Offset: 57h – 54h
Register Name: NonCache Region Register #2 for L1
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address																					REn	Reserved							RSZ		

Bit	Name	Attribute	Description
31-11	BA	R/W	Base Address for the user-defined NonCache Region
10	REn	R/W	Region Enabled for the NonCache Region
9-3	Rsvd	R/W	Reserved
2-0	RSZ	R/W	Size of the NonCache Region Bit 2 Bit 1 Bit 0 Size 0 0 0 2K Bytes 0 0 1 4K Bytes 0 1 0 8K Bytes 0 1 1 16K Bytes 1 0 0 32K Bytes 1 0 1 64K Bytes 1 1 0 128K Bytes 1 1 1 256K Bytes

Register Offset: 5Bh – 58h
Register Name: NonCache Region Register #3 for L1
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address																					En	Reserved							Size		

Bit	Name	Attribute	Description
31-11	BA	R/W	Base Address for the user-defined NonCache Region
10	REn	R/W	Region Enabled for the NonCache Region
9-3	Rsvd	R/W	Reserved
2-0	RSz	R/W	Size of the NonCache Region Bit 2 Bit 1 Bit 0 Size 0 0 0 2K Bytes 0 0 1 4K Bytes 0 1 0 8K Bytes 0 1 1 16K Bytes 1 0 0 32K Bytes 1 0 1 64K Bytes 1 1 0 128K Bytes 1 1 1 256K Bytes

Register Offset: 5Fh – 5Ch
Register Name: NonCache Region Register #4 for L1
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address																					En	Reserved						Size			

Bit	Name	Attribute	Description
31-11	BA	R/W	Base Address for the user-defined NonCache Region
10	REn	R/W	Region Enabled for the NonCache Region
9-4	Rsvd	R/W	Reserved
3-0	RSz	R/W	Size of the NonCache Region Bit 3 Bit 2 Bit 1 Bit 0 Size 0 0 0 0 2K Bytes 0 0 0 1 4K Bytes 0 0 1 0 8K Bytes 0 0 1 1 16K Bytes 0 1 0 0 32K Bytes 0 1 0 1 64K Bytes 0 1 1 0 128K Bytes 0 1 1 1 256K Bytes 1 0 0 0 512K Bytes 1 0 0 1 1M Bytes 1 0 1 0 2M Bytes 1 0 1 1 4M Bytes 1 1 0 0 8M Bytes 1 1 0 1 16M Bytes 1 1 1 0 32M Bytes 1 1 1 1 64M Bytes

Register Offset: 66h
Register Name: Memory Clock Phase Selection Register
Reset Value: 00h

7	6	5	4	3	2	1	0
MCPS_R				MCPS_W			

Bit	Name	Attribute	Description
7-4	MCPS_R	R/W	Memory Clock Phase Selection for Read.
3-0	MCPS_w	R/W	Memory Clock Phase Selection for Write.

Register Offset: 69h – 68h
Register Name: Memory Timing Register
Reset Value: C99Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
tWR	tRC				tRP				tRCD				Reserved		

Bit	Name	Attribute	Description
15	tWR	R/W	SDRAM cycle: Write Recovery Time. 0: 1T 1: 2T
14-11	tRC	R/W	SDRAM cycle: REF/ACT to REF/ACT delay Bit 14 Bit 13 Bit 12 Bit 11 delay period 0 0 0 0 Reserved 0 0 0 1 1 Clock 0 0 1 0 2 Clocks 0 0 1 1 3 Clocks 0 1 0 0 4 Clocks 0 1 0 1 5 Clocks 0 1 1 0 6 Clocks 0 1 1 1 7 Clocks 1 0 0 0 8 Clocks 1 0 0 1 9 Clocks 1 0 1 0 10 Clocks 1 0 1 1 11 Clocks 1 1 0 0 12 Clocks 1 1 0 1 13 Clocks 1 1 1 0 14 Clocks 1 1 1 1 15 Clocks
10-7	tRP	R/W	SDRAM cycle: PRE to ACT command period Bit 10 Bit 9 Bit 8 Bit 7 delay period 0 0 0 0 Reserved 0 0 0 1 1 Clock 0 0 1 0 2 Clocks 0 0 1 1 3 Clocks 0 1 0 0 4 Clocks 0 1 0 1 5 Clocks 0 1 1 0 6 Clocks 0 1 1 1 7 Clocks 1 0 0 0 8 Clocks 1 0 0 1 9 Clocks 1 0 1 0 10 Clocks 1 0 1 1 11 Clocks 1 1 0 0 12 Clocks 1 1 0 1 13 Clocks 1 1 1 0 14 Clocks 1 1 1 1 15 Clocks
6-3	tRCD	R/W	SDRAM cycle: ACT to R/W command delay period Bit 6 Bit 5 Bit 4 Bit 3 delay period 0 0 0 0 Reserved 0 0 0 1 1 Clock 0 0 1 0 2 Clocks 0 0 1 1 3 Clocks 0 1 0 0 4 Clocks 0 1 0 1 5 Clocks 0 1 1 0 6 Clocks 0 1 1 1 7 Clocks

			1 0 0 0 8 Clocks 1 0 0 1 9 Clocks 1 0 1 0 10 Clocks 1 0 1 1 11 Clocks 1 1 0 0 12 Clocks 1 1 0 1 13 Clocks 1 1 1 0 14 Clocks 1 1 1 1 15 Clocks
2-0	Rsvd	RO	Reserved.

Register Offset: 6Bh – 6Ah
Register Name: Memory Control Register
Reset Value: 0004h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												LMR	CasLat		Rsvd

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	LMR	R/W	Lode Mode Register. When this register is written by software, this bit is set by the DRAM controller to program the mode register of SDRAM. After the programming is complete, this bit will be auto-cleared by the DRAM controller. 0: Complete. 1: Programming the mode register of SDRAM.
2-1	CasLat	R/W	SDRAM cycle: Cas Latency Bit 2 Bit 1 delay period 0 0 Reserved 0 1 Reserved 1 0 2 Clocks 1 1 3 Clocks
0	Rsvd	RO	Reserved.

Register Offset: 6Dh – 6Ch
Register Name: Memory Bank Register
Reset Value: 0331h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			C1M	BWT	SS			RAT			BN		CAT		

Bit	Name	Attribute	Description
15-14	Rsvd	RO	Reserved
13	C1M	RW	SDRAM CS_n[1] Mask when set. CS_n[1] is activated when cleared.
12	BWT	RW	SDRAM Data Bus Width Type. 0: 16-bit. 1: Reserved.

11-8	SS	RW	SDRAM Size: Bit 11 Bit 10 Bit 9 Bit 8 SDRAM Size 0 0 0 0 2MB 0 0 0 1 4MB 0 0 1 0 8MB 0 0 1 1 16MB 0 1 0 0 32MB 0 1 0 1 64MB 0 1 1 0 128MB 0 1 1 1 Reserved 1 x x x Reserved
7-5	RAT	RW	SDRAM Row Address Type: Bit 7 Bit 6 Bit 5 No. Bits of Row Address 0 0 0 11 Bits of Row Address 0 0 1 12 Bits of Row Address 0 1 0 13 Bits of Row Address 0 1 1 Reserved 1 x x Reserved
4-3	BN	RW	Bank Number Supported by SDRAM Bit 4 Bit 3 Bank Number 0 0 1 Bank 0 1 2 Banks 1 0 4 Banks 1 1 8 Banks
2-0	CAT	RW	SDRAM Column Address Type: Bit 2 Bit 1 Bit 0 No. Bits of Column Address 0 0 0 8 Bits of Column Address 0 0 1 9 Bits of Column Address 0 1 0 10 Bits of Column Address 0 1 1 11 Bits of Column Address 1 x x Reserved

Register Offset: 6Eh
Register Name: Memory Read/Write Reorder & Refresh Register
Reset Value: 00h

7	6	5	4	3	2	1	0
RWR	Rsvd	RPT					

Bit	Name	Attribute	Description
7	RWR	R/W	Read/Write Reorder Enable 0: Disable 1: Enable
6	Rsvd	RO	Reserved.
5-0	RPT	R/W	Refresh Priority Threshold The R3210 is built in a cumulated refresh counter. When the refresh trigger reaches the threshold, the counter will increase and wait for service to decrease the counter. In order to prevent the Refresh Counter being expired, the system gives highest priority for refresh request to access DRAM when this Refresh Priority Threshold is exceeded.

Register Offset: 70h
Register Name: I/O Cycle Control Register

Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved						PWE	LWE

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved.
1	PWE	R/W	PCI I/O Wait DRAM Write FIFO Empty 0: Disable 1: Enable
0	LWE	R/W	Local I/O Wait DRAM Write FIFO Empty 0: Disable 1: Enable

Register Offset: 72h
Register Name: CPU Decoder Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved							CFD

Bit	Name	Attribute	Description
7-1	Rsvd	RO	Reserved.
0	CFD	R/W	CPU Fast Decode Onboard Cycle 0: Normal 1: Fast

Register Offset: 73h
Register Name: MD/XD Bus Transfer Wait Control Register
Reset Value: 02h

7	6	5	4	3	2	1	0
Reserved					XWS		

Bit	Name	Attribute	Description
7-3	Rsvd	RO	Reserved.
2:0	XWS	R/W	Wait States: 000: 1 wait state 001: 2 wait states 010: 3 wait states 011: 4 wait states 100: 5 wait states 101: 6 wait states 110: 7 wait states 111: 8 wait states

Register Offset: 83h
Register Name: A/B Page Control Register
Reset Value: 08h

7	6	5	4	3	2	1	0
REN	WEN	MRAM		Reserved			

Bit	Name	Attribute	Description
7	REN	R/W	000A0000h-000BFFFFh Read Enable (REN). 0: Disable. 1: Enable. When this bit is disabled, the read requests of memory address 000A0000h-000BFFFFh will be forwarded to the PCI bridge. Otherwise, the read requests of memory address 000A0000h-000BFFFFh are handled based on the MRAM bit of the corresponding requests.
6	WEN	R/W	000A0000h-000BFFFFh Write Enable (SMWEN): 0: Disable. 1: Enable. When this bit is disabled, the write requests of memory address 000A0000h-000BFFFFh will be forwarded to the PCI bridge. Otherwise, the write requests of memory address 000A0000h-000BFFFFh are handled based on the MRAM bit of the corresponding requests.
5-4	MRAM	R/W	Memory Range Access Mode (MRAM[1:0]). 00: PCI Bus. 01: SDRAM. 10: PCI Bus. 11: PCI Bus. The requested handling is based on the code or data references and illustrated in the following table.
3-0	Rsvd	RO	Reserved

Note: *The following table shows the response of requests targeting at 000A0000h-000BFFFFh space*

REN/WEN	Mode (MRAM[1:0])	Code	Data
Disable	Don't care	PCI Bus	PCI Bus
Enable	PCI Bus	PCI Bus	PCI Bus
Enable	SDRAM	SDRAM	SDRAM

Register Offset: 87h – 84h
Register Name: Memory Attribute Register
Reset Value: 0000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd		F0A		ECA		E8A		E4A		E0A		DCA		D8A		D4A		D0A		CCA		C8A		C4A		C0A		Reserved			

Bit	Name	Attribute	Description
31-30	Rsvd	RO	Reserved
29-28	F0A	R/W	Attribute of access to memory address 000F0000h-000FFFFFh Region.

			Bit 29 Bit 28 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
27-26	ECA	R/W	Attribute of access to memory address 000EC000h-000EFFFFh Region. Bit 27 Bit 26 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
25-24	E8A	R/W	Attribute of access to memory address 000E8000h-000EBFFFh Region. Bit 25 Bit 24 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
23-22	E4A	R/W	Attribute of access to memory address 000E4000h-000E7FFFh Region. Bit 23 Bit 22 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
21-20	E0A	RW	Attribute of access to memory address 000E0000h-000E3FFFh Region. Bit 21 Bit 20 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
19-18	DCA	RW	Attribute of access to memory address 000DC000h-000DFFFFh Region. Bit 19 Bit 18 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
17-16	D8A	RW	Attribute of access to memory address 000D8000h-000DBFFFh Region. Bit 17 Bit 16 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
15-14	D4A	RW	Attribute of access to memory address 000D4000h-000D7FFFh Region. Bit 15 Bit 14 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
13-12	D0A	RW	Attribute of access to memory address 000D0000h-000D3FFFh Region. Bit 13 Bit 12 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
11-10	CCA	RW	Attribute of access to memory address 000CC000h-000CFFFFh Region. Bit 11 Bit 10 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
9-8	C8A	RW	Attribute of access to memory address 000C8000h-000CBFFFh Region. Bit 9 Bit 8 Description

			0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
7-6	C4A	RW	Attribute of access to memory address 000C4000h-000C7FFFh Region. Bit 7 Bit 6 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
5-4	C0A	RW	Attribute of access to memory address 000C0000h-000C3FFFh Region. Bit 5 Bit 4 Description 0 0 Read/Write from/to PCI Bus 0 1 Read from SDRAM, Write to PCI Bus 1 0 Read from PCI Bus, Write to SDRAM 1 1 Read/Write from/to SDRAM
3-0	Rsvd	RW	Reserved

Register Offset: 93h – 90h
Register Name: Customer ID Register
Reset Value: 00321000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CID																															

Bit	Name	Attribute	Description
31-0	CID	RO	Customer ID.

Register Offset: 97h – 94h
Register Name: Spare 1 Register
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S1																															

Bit	Name	Attribute	Description
31-0	S1	R/W	Store Data. These registers can be used by BIOS to store temporary data.

Register Offset: 9Bh – 98h
Register Name: Spare 2 Register
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

S2

Bit	Name	Attribute	Description
31-0	S2	R/W	Store Data. These registers can be used by BIOS to store temporary data.

Register Offset: 9Fh – 9Ch
Register Name: Spare 3 Register
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S3																															

Bit	Name	Attribute	Description
31-0	S3	R/W	Store Data. These registers can be used by BIOS to store temporary data.

Register Offset: C3h – C0h
Register Name: USB Control Register
Reset Value: 0000_0000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd					PCR											PBE	PBO	PBC		Rsvd		PBF	PBD	FBE	Rsvd			FBS		FBF	FBD

Bit	Name	Attribute	Description
31-30	Rsvd	RO	Reserved.
29-16	PCR	R/W	USB PHY Control Register.
15	PBE	R/W	USB PHY Bist Enable when set.
14	PBO	R/W	USB PHY Bist Out. 0:port1 results in bit9. 1:port2 results in bit9
13-12	PBC	R/W	USB PHY Bist Current. 01b: BIST test port1. 10b: BIST test port2
11-10	Rsvd	RO	Reserved.
9	PBF	RO	USB PHY Bist Fault when set.
8	PBD	RO	USB PHY Bist Done when set.
7	FBE	R/W	USB FIFO Bist Enable when set.
6-4	Rsvd	RO	Reserved.
3-2	FBS	RO	USB FIFO Bist Status.
1	FBF	RO	USB FIFO Bist Fault.

0	FBD	RO	USB FIFO Bist Done.

11.3.2 R3210 South Bridge Configuration Registers

Register Offset: 01h – 00h
Register Name: Vendor ID Register
Reset Value: 17F3h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VID															

Bit	Name	Attribute	Description
15-0	VID	RO	This register contains a 16-bit value assigned to RDC Semiconductor Co., Ltd. If the R3210 Configuration Register Index 41 Bit 0 = ’1’, this register can be read and written. Otherwise, this register is Read-Only. BIOS should be used to program a value to this register and then lock it by setting the R3210 Configuration Register Index 41 Bit 0 = ’0’.

Register Offset: 03h – 02h
Register Name: Device ID Register
Reset Value: 6030h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID															

Bit	Name	Attribute	Description
15-0	DID	RO	This register contains a 16-bit value to specify a particular device. If the R3210 Configuration Register Index 41 Bit 0 = ’1’, this register can be read and written. Otherwise, this register is Read-Only. BIOS should be used to program a value to this register and then lock it by setting the R3210 Configuration Register Index 41 Bit 0 = ’0’.

Register Offset: 05h – 04h
Register Name: Command Register
Reset Value: 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SFE	Reserved			MWI	SCOC	PMDC	MSAC	IOSAC

Bit	Name	Attribute	Description
15-9	Rsvd	RO	Reserved. These bits always return ’0’s.
8	SFE	R/W	SERR_n Function Enable/Disable 0: Disabled.

			1: Enabled.
7-5	Rsvd	RO	Reserved. These bits always return ’0’s.
4	MWI	R/W	Memory Write and Invalid Command. This bit always returns ‘0’.
3	SCOC	R/W	Special Cycle operation control. This bit always returns ‘1’.
2	PMDC	R/W	PCI Bus Master Device Control. This bit always returns ‘1’.
1	MSAC	R/W	Memory Space Access Control. This bit always returns ‘1’.
0	IOSAC	R/W	I/O Space Access Control. This bit always returns ‘1’.

Register Offset: 07h – 06h
Register Name: Status Register
Reset Value: 0400h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	SS	RMAS	RTAS	STAS	DT		Reserved								

Bit	Name	Attribute	Description
15	DPE	RO	Detected Parity Error. This bit must be set whenever the device detects a parity error. This is a read only bit and is cleared by writing '1' to it.
14	SS	RO	SERR_n Status. This bit must be set whenever the device asserts SERR_n. This is a read only bit and is cleared by writing '1' to it.
13	RMAS	RO	Receive Master Abort Status when the R3210 acts as a master. This bit is set to '1' when the R3210 generates a transaction (Except for Special Cycle), and is terminated with master-abort. This is a read only bit and is cleared by writing '1' to it.
12	RTAS	RO	Receive Target Abort Status when the R3210 acts as a master. This bit is set to '1' when the R3210 encounters a target abort condition. This is a read only bit and is cleared by writing a '1' to it.
11	STAS	RO	Signal Target Abort Status when the R3210 acts as a slave. The R3210 as a slave never generates a Target abort. This bit is always 0.
10-9	DT	RO	DEVSEL_n Timing. The R3210 always generates DEVSEL_n with low timing. These bits are always ‘11’.
8-0	Rsvd	RO	Reserved. These bits always return ’0’s.

Register Offset: 08h
Register Name: Revision ID Register
Reset Value: 00h

7	6	5	4	3	2	1	0
RID							

Bit	Name	Attribute	Description
7-0	RID	R/W	Version number of the R3210. If the R3210 Configuration Register Index 41 Bit 0 = ’1’, this register can be read and written. Otherwise, this register is Read-Only. BIOS should be used to program a value to this register and then lock it by setting the R3210 Configuration Register Index 41 Bit 0 = ’0’.

Register Offset: 0Bh – 09h
Register Name: Class Code Register
Reset Value: 060100h

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC																							

Bit	Name	Attribute	Description
23-0	CC	RO	Class Code of the R3210.

Register Offset: 0Eh
Register Name: Header Type Register
Reset Value: 00h

7	6	5	4	3	2	1	0
HT							

Bit	Name	Attribute	Description
7-0	HT	RO	This register identifies the type of predefined header in the configuration space. Since the R3210 is a single function device (bit7='0') and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Offset: 2Dh – 2Ch
Register Name: Subsystem Vendor ID Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVID															

Bit	Name	Attribute	Description
15-0	SVID	R/WL	This register contains the subsystem Vendor ID. If the R3210 Configuration Register Index 41 Bit 0 = '1', this register can be read and written. Otherwise, this register is Read-Only. BIOS should be used to program a value to this register and then lock it by setting the R3210 Configuration Register Index 41 Bit 0 = '0'.

Register Offset: 2Fh – 2Eh
Register Name: Subsystem Device ID Register
Reset Value: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SDID

Bit	Name	Attribute	Description
15-0	SDID	R/WL	This register contains the subsystem Device ID. If the R3210 Configuration Register Index 41 Bit 0 = '1', this register can be read and written. Otherwise, this register is Read-Only. BIOS should be used to program a value to this register and then lock it by setting the R3210 Configuration Register Index 41 Bit 0 = '0'.

Register Offset: 40h
Register Name: Boot Strapping Register
Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved						FRS	

Bit	Name	Attribute	Description
7-2	Rsvd	RO	Reserved
1-0	FRS	RO	X Bus/LPC/FWH Flash ROM Selected 00: 8-bit Flash ROM is located on X Bus 01: 16-bit Flash ROM is located on X Bus 10: Flash ROM is located on LPC 11: Flash ROM is located on LPC/FWH These two bits reflect the boot strapping state of ROMTYPE[1:0] pins on the rising edge of system reset. Pulling down ROMTYPE[1:0] pins on the rising edge of system reset will set the corresponding bit to '0'. Pulling up ROMTYPE[1:0] pins on the rising edge of system reset will set the corresponding bit to '1'.

Register Offset: 41h
Register Name: Write Lock and LPC Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
Rsvd			SRC	DOCS	P92FE	P92S	LB

Bit	Name	Attribute	Description
7-5	Rsvd	RO	Reserved
4	SRC	R/W	PCI Soft Reset Control. 0: When the CPU soft reset is initialized, PCIRST_n will not be active. 1: When the CPU soft reset is initialized, PCIRST_n will be active. This bit is used to control the assertion of PCIRST_n when the CPU soft reset is initialized. It may be necessary to reset some PCI cards during the CPU soft reset. BIOS can use this bit to solve this issue by resetting the whole PCI bus.
3	DOCS	R/W	DMA Operating Clock Selected. 0: 4 MHz 1: 8 MHz
2	P92FE	R/W	Internal port 92 Write Function Enable/Disable 0: Disable 1: Enable This bit is no effect when bit 1 of this register is set to '0'

1	P92S	R/W	Internal/LPC Port 92h Selection 0: LPC Port 92h Selected 1: Internal Port 92h Selected
0	LB	R/W	R3210 Vendor ID, System ID and Revision ID Registers Read Only Control. 0: Read only. 1: Read/Write.

Register Offset: 43h – 42h
Register Name: Flash ROM Chip Select Control Register
Reset Value: 0000h

15	14 13	12 11 10 9 8 7 6 5 4 3 2	1	0
FRWPM	Reserved	Reserved	FRR2	FRR1

Bit	Name	Attribute	Description
15	FRWPM	R/W	Flash ROM Write Protect Mode. 0: Write Disable. 1: Write Enable. When this bit is '0', ROMCS_n will be asserted only in memory read cycle. When this bit is '1', ROMCS_n will be asserted in memory read/write cycles.
14-13	Rsvd	RO	Reserved
12-2	Rsvd	R / W	Reserved. These bits must be set "1".
1	FRR2	R/W	Flash ROM Region 2 (000C0000h-000DFFFFh) for ROMCS_n Decode 0: Disable. 1: Enable.
0	FRR1	R/W	Flash ROM Region 1 for ROMCS_n Decode. 0: 000F0000h-000FFFFFh and FFFF0000h-FFFFFFFFh 1: 000E0000h-000FFFFFh and FFFE0000h-FFFFFFFFh

Register Offset: 46h – 44h
Register Name: Watchdog Timer Control
Reset Value: 000002h

23	22 21 20	19	18	17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
WTE	WTI	RF	NF	WIF	Reserved	IRT	WC

Bit	Name	Attribute	Description
23	WTE	R/W	Enable/Disable Watchdog Timer 0: Disable 1: Enable
22-21	WTI	R/W	Generate a CPU Reset/NMI/WDT IRQ when WDT Timeout is reached 00: WDT generates a CPU reset when WDT timeout is reached. 01: WDT generates an NMI interrupt when WDT timeout is reached and NMI flag bit (Bit 19) is set to '0'. And WDT generates a CPU reset when WDT timeout is reached and NMI flag bit (Bit 19) is set to '1' 10: WDT generates a WDT IRQ when WDT timeout is reached and WDT IRQ flag bit (Bit 18) is set to '0'. And WDT generates a CPU reset when WDT timeout is reached and WDT IRQ flag

<table>
<tr><td></td><td></td><td></td><td>bit (Bit 18) is set to ‘1’
11: Reserved</td></tr>
<tr><td>20</td><td>RF</td><td>R/W</td><td>Reset Flag
This bit will be set to ‘1’ when the WDT reset event has occurred. Write ‘1’ to this bit to clear Reset Flag bit to ‘0’</td></tr>
<tr><td>19</td><td>NF</td><td>R/W</td><td>NMI Flag
This bit will be set to ‘1’ when the WDT NMI interrupt event has occurred. Write ‘1’ to this bit to clear NMI Flag bit to ‘0’</td></tr>
<tr><td>18</td><td>WIF</td><td>R/W</td><td>WDT IRQ Flag
This bit will be set to ‘1’ when the WDT IRQ interrupt event has occurred. Write ‘1’ to this bit to clear WDT IRQ Flag bit to ‘0’</td></tr>
<tr><td>17-12</td><td>Rsvd</td><td>RO</td><td>Reserved</td></tr>
<tr><td>11-8</td><td>IRT</td><td>R/W</td><td>WDT IRQ Routing Table
Bit11 Bit10 Bit9 Bit8 Routing Table
0 0 0 0 Disable.
0 0 0 1 IRQ[9]
0 0 1 0 IRQ[3]
0 0 1 1 IRQ[10]
0 1 0 0 IRQ[4]
0 1 0 1 IRQ[5]
0 1 1 0 IRQ[7]
0 1 1 1 IRQ[6]
1 0 0 0 IRQ[1]
1 0 0 1 IRQ[11]
1 0 1 0 Reserved
1 0 1 1 IRQ[12]
1 1 0 0 Reserved
1 1 0 1 IRQ[14]
1 1 1 0 Reserved
1 1 1 1 IRQ[15]
These four bits are used to route WDT IRQ to any 8259 Interrupt lines. The BIOS should be used to inhibit the setting of the reserved value.</td></tr>
<tr><td>7-0</td><td>WC</td><td>R/W</td><td>WDT Count. The Count Setting determines the duration of the WDT Timeout Internal
a. The duration equation: $2^{Exponent}$/Frequency
b. The exponent of Count setting:
Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Exponent
0 0 0 0 0 0 0 0 N/A
x x x x x x x 1 10
x x x x x x 1 0 20
x x x x x 1 0 0 21
x x x x 1 0 0 0 22
x x x 1 0 0 0 0 23
x x 1 0 0 0 0 0 24
x 1 0 0 0 0 0 0 25
1 0 0 0 0 0 0 0 26
c. Frequency: 14.318MHz (external) or 12.5MHz (internal)

WDT Timer Duration Reference Table:
<table>
<tr><th>Frequency\ Exponent</th><th>10</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th></tr>
<tr><td>14.318MHz</td><td>71.5 us</td><td>73.2 ms</td><td>146 ms</td><td>293 ms</td><td>586 ms</td><td>1.17 s</td><td>2.34 s</td><td>4.69 s</td></tr>
<tr><td>12.5MHz</td><td>81.92 us</td><td>83.9 ms</td><td>167.8 ms</td><td>335.5 ms</td><td>671.1 ms</td><td>1.34 s</td><td>2.68 s</td><td>5.37 s</td></tr>
</table></td></tr>
</table>

Register Offset: 4Bh – 48h
Register Name: General-Purpose I/O Control Register I
Reset Value: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G31E	G30E	G29E	G28E	G27E	G26E	G25E	G24E	G23E	G22E	G21E	G20E	G19E	G18E	G17E	G16E	G15E	G14E	G13E	G12E	G11E	G10E	G9E	G8E	G7E	G6E	G5E	G4E	G3E	G2E	G1E	G0E

Bit	Name	Attribute	Description
31	G31E	R/W	GPIO31 Function Enable/Disable. 0: Disable. This pin operates in normal (SA15) function. 1: Enable. This pin operates as GPIO31 with an internal 75KΩ pull-up resistor.
30	G30E	R/W	GPIO30 Function Enable/Disable. 0: Disable. This pin operates in normal (SA14) function. 1: Enable. This pin operates as GPIO30 with an internal 75KΩ pull-up resistor.
29	G29E	R/W	GPIO29 Function Enable/Disable. 0: Disable. This pin operates in normal (SA13) function. 1: Enable. This pin operates as GPIO29 with an internal 75KΩ pull-up resistor.
28	G28E	R/W	GPIO28 Function Enable/Disable. 0: Disable. This pin operates in normal (PGNT2_n) function. 1: Enable. This pin operates as GPIO28 with an internal 75KΩ pull-up resistor.
27	G27E	R/W	GPIO27 Function Enable/Disable. 0: Disable. This pin operates in normal (PGNT1_n) function. 1: Enable. This pin operates as GPIO27 with an internal 75KΩ pull-up resistor.
26	G26E	R/W	GPIO26 Function Enable/Disable. 0: Disable. This pin operates in normal (PGNT0_n) function. 1: Enable. This pin operates as GPIO26 with an internal 75KΩ pull-up resistor.
25	G25E	R/W	GPIO25 Function Enable/Disable. 0: Disable. This pin operates in normal (PREQ2_n) function. 1: Enable. This pin operates as GPIO25 with an internal 75KΩ pull-up resistor.
24	G24E	R/W	GPIO24 Function Enable/Disable. 0: Disable. This pin operates in normal (PREQ1_n) function. 1: Enable. This pin operates as GPIO24 with an internal 75KΩ pull-up resistor.
23	G23E	R/W	GPIO23 Function Enable/Disable. 0: Disable. This pin operates in normal (PREQ0_n) function. 1: Enable. This pin operates as GPIO23 with an internal 75KΩ pull-up resistor.
22	G22E	R/W	GPIO22 Function Enable/Disable. 0: Disable. This pin operates in normal (INTD_n) function. 1: Enable. This pin operates as GPIO22 with an internal 75KΩ pull-up resistor.
21	G21E	R/W	GPIO21 Function Enable/Disable. 0: Disable. This pin operates in normal (INTC_n) function. 1: Enable. This pin operates as GPIO21 with an internal 75KΩ pull-up resistor.
20	G20E	R/W	GPIO20 Function Enable/Disable. 0: Disable. This pin operates in normal (INTB_n) function. 1: Enable. This pin operates as GPIO20 with an internal 75KΩ pull-up resistor.
19	G19E	R/W	GPIO19 Function Enable/Disable. 0: Disable. This pin operates in normal (INTA_n) function. 1: Enable. This pin operates as GPIO19 with an internal 75KΩ pull-up resistor.
18	G18E	R/W	GPIO18 Function Enable/Disable. 0: Disable. This pin operates in normal (IRQ8_n) function. 1: Enable. This pin operates as GPIO18 with an internal 75KΩ pull-up resistor.
17	G17E	R/W	GPIO17 Function Enable/Disable. 0: Disable. This pin operates in normal (RTCWR) function. 1: Enable. This pin operates as GPIO17 with an internal 75KΩ pull-up resistor.

16	G16E	R/W	GPIO16 Function Enable/Disable. 0: Disable. This pin operates in normal (RTCRD) function. 1: Enable. This pin operates as GPIO16 with an internal 75KΩ pull-up resistor.
15	G15E	R/W	GPIO15 Function Enable/Disable. 0: Disable. This pin operates in normal (RTCAS) function. 1: Enable. This pin operates as GPIO15 with an internal 75KΩ pull-up resistor.
14	G14E	R/W	GPIO14 Function Enable/Disable. 0: Disable. This pin operates in normal (RI_n) function. 1: Enable. This pin operates as GPIO14 with an internal 75KΩ pull-up resistor.
13	G13E	R/W	GPIO13 Function Enable/Disable. 0: Disable. This pin operates in normal (DCD_n/TDI) function. 1: Enable. This pin operates as GPIO13 with an internal 75KΩ pull-up resistor.
12	G12E	R/W	GPIO12 Function Enable/Disable. 0: Disable. This pin operates in normal (DSR_n/TCK) function. 1: Enable. This pin operates as GPIO12 with an internal 75KΩ pull-up resistor.
11	G11E	R/W	GPIO11 Function Enable/Disable. 0: Disable. This pin operates in normal (CTS_n/TMS) function. 1: Enable. This pin operates as GPIO11 with an internal 75KΩ pull-up resistor.
10	G10E	R/W	GPIO10 Function Enable/Disable. 0: Disable. This pin operates in normal (DTR_n) function. 1: Enable. This pin operates as GPIO10 with an internal 75KΩ pull-up resistor.
9	G9E	R/W	GPIO9 Function Enable/Disable. 0: Disable. This pin operates in normal (RTS_n/TDO) function. 1: Enable. This pin operates as GPIO9 with an internal 75KΩ pull-up resistor.
8	G8E	R/W	GPIO8 Function Enable/Disable. 0: Disable. This pin operates in normal (SOUT) function. 1: Enable. This pin operates as GPIO8 with an internal 75KΩ pull-up resistor.
7	G7E	R/W	GPIO7 Function Enable/Disable. 0: Disable. This pin operates in normal (SIN) function. 1: Enable. This pin operates as GPIO7 with an internal 75KΩ pull-up resistor.
6	G6E	R/W	GPIO6 Function Enable/Disable. 0: Disable. This pin operates in normal (IRQSER) function. 1: Enable. This pin operates as GPIO6 with an internal 75KΩ pull-up resistor.
5	G5E	R/W	GPIO5 Function Enable/Disable. 0: Disable. This pin operates in normal (LDRQ_n) function. 1: Enable. This pin operates as GPIO5 with an internal 75KΩ pull-up resistor.
4	G4E	R/W	GPIO4 Function Enable/Disable. 0: Disable. This pin operates in normal (LFRAME_n) function. 1: Enable. This pin operates as GPIO4 with an internal 75KΩ pull-up resistor.
3	G3E	R/W	GPIO3 Function Enable/Disable. 0: Disable. This pin operates in normal (LAD3) function. 1: Enable. This pin operates as GPIO3 with an internal 75KΩ pull-up resistor.
2	G2E	R/W	GPIO2 Function Enable/Disable. 0: Disable. This pin operates in normal (LAD2) function. 1: Enable. This pin operates as GPIO2 with an internal 75KΩ pull-up resistor.
1	G1E	R/W	GPIO1 Function Enable/Disable. 0: Disable. This pin operates in normal (LAD1) function. 1: Enable. This pin operates as GPIO1 with an internal 75KΩ pull-up resistor.
0	G0E	R/W	GPIO0 Function Enable/Disable. 0: Disable. This pin operates in normal (LAD0) function. 1: Enable. This pin operates as GPIO0 with an internal 75KΩ pull-up resistor.

Register Offset: 4Fh – 4Ch
Register Name: General-Purpose I/O Data Register I
Reset Value: FFFFFFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G31D	G30D	G29D	G28D	G27D	G26D	G25D	G24D	G23D	G22D	G21D	G20D	G19D	G18D	G17D	G16D	G15D	G14D	G13D	G12D	G11D	G10D	G9D	G8D	G7D	G6D	G5D	G4D	G3D	G2D	G1D	G0D

Bit	Name	Attribute	Description
31	G31D	R/W	GPIO31 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO31 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO31 pin to ‘High’. In Input Mode: Read input data of GPIO31 from this bit. ‘1’ means that the external device drives the GPIO31 pin to ‘High’, and ‘0’ means that the external device drives GPIO31 to ‘Low’. A ‘1’ must be written to this bit when GPIO31 is in Input Mode.
30	G30D	R/W	GPIO30 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO30 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO30 pin to ‘High’. In Input Mode: Read input data of GPIO30 from this bit. ‘1’ means that the external device drives the GPIO30 pin to ‘High’, and ‘0’ means that the external device drives GPIO30 to ‘Low’. A ‘1’ must be written to this bit when GPIO30 is in Input Mode.
29	G29D	R/W	GPIO29 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO29 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO29 pin to ‘High’. In Input Mode: Read input data of GPIO29 from this bit. ‘1’ means that the external device drives the GPIO29 pin to ‘High’, and ‘0’ means that the external device drives GPIO29 to ‘Low’. A ‘1’ must be written to this bit when GPIO29 is in Input Mode.
28	G28D	R/W	GPIO28 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO28 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO28 pin to ‘High’. In Input Mode: Read input data of GPIO28 from this bit. ‘1’ means that the external device drives the GPIO28 pin to ‘High’, and ‘0’ means that the external device drives GPIO28 to ‘Low’. A ‘1’ must be written to this bit when GPIO28 is in Input Mode.
27	G27D	R/W	GPIO27 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO27 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO27 pin to ‘High’. In Input Mode: Read input data of GPIO27 from this bit. ‘1’ means that the external device drives the GPIO27 pin to ‘High’, and ‘0’ means that the external device drives GPIO27 to ‘Low’. A ‘1’ must be written to this bit when GPIO27 is in Input Mode.
26	G26D	R/W	GPIO26 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO26 pin to ‘Low’. Write ‘1’ to this bit to drive theGPIO26 pin to ‘High’. In Input Mode: Read input data of GPIO26 from this bit. ‘1’ means that the external device drives the GPIO26 pin to ‘High’, and ‘0’ means that the external device drives GPIO26 to ‘Low’. A ‘1’ must be written to this bit when GPIO26 is in Input Mode.
25	G25D	R/W	GPIO25 Control/Data

			In Output Mode: Write '0' to this bit to drive the GPIO25 pin to 'Low'. Write '1' to this bit to drive the GPIO25 pin to 'High'. In Input Mode: Read input data of GPIO25 from this bit. '1' means that the external device drives the GPIO25 pin to 'High', and '0' means that the external device drives GPIO25 to 'Low'. A '1' must be written to this bit when GPIO25 is in Input Mode.
24	G24D	R/W	GPIO24 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO24 pin to 'Low'. Write '1' to this bit to drive the GPIO24 pin to 'High'. In Input Mode: Read input data of GPIO24 from this bit. '1' means that the external device drives the GPIO24 pin to 'High', and '0' means that the external device drives GPIO24 to 'Low'. A '1' must be written to this bit when GPIO24 is in Input Mode.
23	G23D	R/W	GPIO23 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO23 pin to 'Low'. Write '1' to this bit to drive the GPIO23 pin to 'High'. In Input Mode: Read input data of GPIO23 from this bit. '1' means that the external device drives the GPIO23 pin to 'High', and '0' means that the external device drives GPIO23 to 'Low'. A '1' must be written to this bit when GPIO23 is in Input Mode.
22	G22D	R/W	GPIO22 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO22 pin to 'Low'. Write '1' to this bit to drive the GPIO22 pin to 'High'. In Input Mode: Read input data of GPIO22 from this bit. '1' means that the external device drives the GPIO22 pin to 'High', and '0' means that the external device drives GPIO22 to 'Low'. A '1' must be written to this bit when GPIO22 is in Input Mode.
21	G21D	R/W	GPIO21 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO21 pin to 'Low'. Write '1' to this bit to drive the GPIO21 pin to 'High'. In Input Mode: Read input data of GPIO21 from this bit. '1' means that the external device drives the GPIO21 pin to 'High', and '0' means that the external device drives GPIO21 to 'Low'. A '1' must be written to this bit when GPIO21 is in Input Mode.
20	G20D	R/W	GPIO20 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO20 pin to 'Low'. Write '1' to this bit to drive the GPIO20 pin to 'High'. In Input Mode: Read input data of GPIO20 from this bit. '1' means that the external device drives the GPIO20 pin to 'High', and '0' means that the external device drives GPIO20 to 'Low'. A '1' must be written to this bit when GPIO20 is in Input Mode.
19	G19D	R/W	GPIO19 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO19 pin to 'Low'. Write '1' to this bit to drive the GPIO19 pin to 'High'. In Input Mode: Read input data of GPIO19 from this bit. '1' means that the external device drives the GPIO19 pin to 'High', and '0' means that the external device drives GPIO19 to 'Low'. A '1' must be written to this bit when GPIO19 is in Input Mode.
18	G18D	R/W	GPIO18 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO18 pin to 'Low'. Write '1' to this bit to drive theGPIO18 pin to 'High'. In Input Mode: Read input data of GPIO18 from this bit. '1' means that the external device drives the

			GPIO18 pin to 'High', and '0' means that the external device drives GPIO18 to 'Low'. A '1' must be written to this bit when GPIO18 is in Input Mode.
17	G17D	R/W	GPIO17 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO17 pin to 'Low'. Write '1' to this bit to drive the GPIO17 pin to 'High'. In Input Mode: Read input data of GPIO17 from this bit. '1' means that the external device drives the GPIO17 pin to 'High', and '0' means that the external device drives GPIO17 to 'Low'. A '1' must be written to this bit when GPIO17 is in Input Mode.
16	G16D	R/W	GPIO16 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO16 pin to 'Low'. Write '1' to this bit to drive the GPIO16 pin to 'High'. In Input Mode: Read input data of GPIO16 from this bit. '1' means that the external device drives the GPIO16 pin to 'High', and '0' means that the external device drives GPIO16 to 'Low'. A '1' must be written to this bit when GPIO16 is in Input Mode.
15	G15D	R/W	GPIO15 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO15 pin to 'Low'. Write '1' to this bit to drive the GPIO15 pin to 'High'. In Input Mode: Read input data of GPIO15 from this bit. '1' means that the external device drives the GPIO15 pin to 'High', and '0' means that the external device drives GPIO15 to 'Low'. A '1' must be written to this bit when GPIO15 is in Input Mode.
14	G14D	R/W	GPIO14 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO14 pin to 'Low'. Write '1' to this bit to drive the GPIO14 pin to 'High'. In Input Mode: Read input data of GPIO14 from this bit. '1' means that the external device drives the GPIO14 pin to 'High', and '0' means that the external device drives GPIO14 to 'Low'. A '1' must be written to this bit when GPIO14 is in Input Mode.
13	G13D	R/W	GPIO13 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO13 pin to 'Low'. Write '1' to this bit to drive the GPIO13 pin to 'High'. In Input Mode: Read input data of GPIO13 from this bit. '1' means that the external device drives the GPIO13 pin to 'High', and '0' means that the external device drives GPIO13 to 'Low'. A '1' must be written to this bit when GPIO13 is in Input Mode.
12	G12D	R/W	GPIO12 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO12 pin to 'Low'. Write '1' to this bit to drive the GPIO12 pin to 'High'. In Input Mode: Read input data of GPIO12 from this bit. '1' means that the external device drives the GPIO12 pin to 'High', and '0' means that the external device drives GPIO12 to 'Low'. A '1' must be written to this bit when GPIO12 is in Input Mode.
11	G11D	R/W	GPIO11 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO11 pin to 'Low'. Write '1' to this bit to drive the GPIO11 pin to 'High'. In Input Mode: Read input data of GPIO11 from this bit. '1' means that the external device drives the GPIO11 pin to 'High', and '0' means that the external device drives GPIO11 to 'Low'. A '1' must be written to this bit when GPIO11 is in Input Mode.
10	G10D	R/W	GPIO10 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO10 pin to 'Low'. Write '1' to this bit to drive the GPIO10

			pin to 'High'. In Input Mode: Read input data of GPIO10 from this bit. '1' means that the external device drives the GPIO10 pin to 'High', and '0' means that the external device drives GPIO10 to 'Low'. A '1' must be written to this bit when GPIO10 is in Input Mode.
9	G9D	R/W	GPIO9 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO9 pin to 'Low'. Write '1' to this bit to drive the GPIO9 pin to 'High'. In Input Mode: Read input data of GPIO9 from this bit. '1' means that the external device drives the GPIO9 pin to 'High', and '0' means that the external device drives GPIO9 to 'Low'. A '1' must be written to this bit when GPIO9 is in Input Mode.
8	G8D	R/W	GPIO8 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO8 pin to 'Low'. Write '1' to this bit to drive the GPIO8 pin to 'High'. In Input Mode: Read input data of GPIO8 from this bit. '1' means that the external device drives the GPIO8 pin to 'High', and '0' means that the external device drives GPIO8 to 'Low'. A '1' must be written to this bit when GPIO8 is in Input Mode.
7	G7D	R/W	GPIO7 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO7 pin to 'Low'. Write '1' to this bit to drive the GPIO7 pin to 'High'. In Input Mode: Read input data of GPIO7 from this bit. '1' means that the external device drives the GPIO7 pin to 'High', and '0' means that the external device drives GPIO7 to 'Low'. A '1' must be written to this bit when GPIO7 is in Input Mode.
6	G6D	R/W	GPIO6 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO6 pin to 'Low'. Write '1' to this bit to drive the GPIO6 pin to 'High'. In Input Mode: Read input data of GPIO6 from this bit. '1' means that the external device drives the GPIO6 pin to 'High', and '0' means that the external device drives GPIO6 to 'Low'. A '1' must be written to this bit when GPIO6 is in Input Mode.
5	G5D	R/W	GPIO5 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO5 pin to 'Low'. Write '1' to this bit to drive the GPIO5 pin to 'High'. In Input Mode: Read input data of GPIO5 from this bit. '1' means that the external device drives the GPIO5 pin to 'High', and '0' means that the external device drives GPIO5 to 'Low'. A '1' must be written to this bit when GPIO5 is in Input Mode.
4	G4D	R/W	GPIO4 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO4 pin to 'Low'. Write '1' to this bit to drive the GPIO4 pin to 'High'. In Input Mode: Read input data of GPIO4 from this bit. '1' means that the external device drives the GPIO4 pin to 'High', and '0' means that the external device drives GPIO4 to 'Low'. A '1' must be written to this bit when GPIO4 is in Input Mode.
3	G3D	R/W	GPIO3 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO3 pin to 'Low'. Write '1' to this bit to drive the GPIO3 pin to 'High'. In Input Mode: Read input data of GPIO3 from this bit. '1' means that the external device drives the GPIO3 pin to 'High', and '0' means that the external device drives GPIO3 to 'Low'. A '1' must be written to this bit when GPIO3 is in Input Mode.

2	G2D	R/W	GPIO2 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO2 pin to 'Low'. Write '1' to this bit to drive the GPIO2 pin to 'High'. In Input Mode: Read input data of GPIO2 from this bit. '1' means that the external device drives the GPIO2 pin to 'High', and '0' means that the external device drives GPIO2 to 'Low'. A '1' must be written to this bit when GPIO2 is in Input Mode.
1	G1D	R/W	GPIO1 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO1 pin to 'Low'. Write '1' to this bit to drive the GPIO1 pin to 'High'. In Input Mode: Read input data of GPIO1 from this bit. '1' means that the external device drives the GPIO1 pin to 'High', and '0' means that the external device drives GPIO1 to 'Low'. A '1' must be written to this bit when GPIO1 is in Input Mode.
0	G0D	R/W	GPIO0 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO0 pin to 'Low'. Write '1' to this bit to drive the GPIO0 pin to 'High'. In Input Mode: Read input data of GPIO0 from this bit. '1' means that the external device drives the GPIO0 pin to 'High', and '0' means that the external device drives GPIO0 to 'Low'. A '1' must be written to this bit when GPIO0 is in Input Mode.

Register Offset: 50h

Register Name: Serial IRQ (IRQSER) Control Register

Reset Value: 12h

7	6	5	4	3	2	1	0
SIE	SPFPW	IFN					STFPW

Bit	Name	Attribute	Description
7	SIE	R/W	Serial IRQ (IRQSER) Enable/Disable 0: Disable; 1: Enable. To enable the Serial IRQ, follow the programming sequences: 1. Program Bit 6 of this register first to enable the continuous mode repetition. 2. Program this bit to enable the Serial IRQ function.
6	SPFPW	R/W	Stop Frame Pulse Width. This Stop Frame Pulse Width is used to decide what kind of mode will be entered from next cycle. 0: 2 PCICLK (Quiet Mode). 1: 3 PCICLK (Continuous Mode).
5-2	IFN	R/W	Number of IRQ/Data Frames. 0000: 17 Slots. 0001: 18 Slots. 0010: 19 Slots. 0011: 20 Slots. 0100: 21 Slots. (default recommended for BIOS setting) 0101-1111: reserved. These four bits are used to define the number of IRQ/Data Frame Slots (PCICLK). 21 Slots are recommended for BIOS setting.
1-0	STFPW	R/W	Start Frame Pulse Width. 00: 4 PCICLK. 01: 6 PCICLK. 10: 8 PCICLK 11: Reserved. These two bits are used to select the Start Frame pulse width from 4 PCICLK to 8 PCICLK. 8 PCICLK are recommended when the R3210 resides in Primary PCI bus. For some special applications, when the R3210 does not reside in Primary PCI bus, 6 PCICLK are

			recommended.

Register Offset: 51h
Register Name: LPC Control Register
Reset Value: 10h

7	6	5	4	3	2	1	0
Reserved			PPDC		ICME	Rsvd	LIC

Bit	Name	Attribute	Description
7-5	Rsvd	RO	Reserved
4-3	PPDC	R/W	3.3/5.0V PAD Pull Up/Down control register, for next version. 01: PULL DOWN 10: PULL UP Other: NONE
2	ICME	R/W	Repeat Serial IRQ Continuous Mode Enable/Disable. 0: Disable. 1: Enable. This bit is used to enable the Serial IRQ Continuous mode repetition. This bit must be enabled when the Serial IRQ function is enabled.
1	Rsvd	RO	Reserved
0	LIC	R/W	LPC Interface Control. 0: Disable LPC function if bit 1 of Boot Strapping Register is a '0'. Otherwise, LPC function is enabled 1: Enable LPC function.

Register Offset: 52h
Register Name: LPC Legacy COM Port Decoding Register
Reset Value: 00h

7	6	5	4	3	2	1	0
DP7E	DP6E	DP5E	DP4E	DP3E	DP2E	DP1E	DP0E

Bit	Name	Attribute	Description
7	DP7E	R/W	Enable/Disable Decode Port 3F8h-3FFh (COM1) as an LPC Access 0: Disable 1: Enable
6	DP6E	R/W	Enable/Disable Decode Port 3E8h-3EFh (COM3) as an LPC Access 0: Disable 1: Enable
5	DP5E	R/W	Enable/Disable Decode Port 338h-33Fh as an LPC Access 0: Disable 1: Enable
4	DP4E	R/W	Enable/Disable Decode Port 2F8h-2FFh (COM2) as an LPC Access 0: Disable 1: Enable
3	DP3E	R/W	Enable/Disable Decode Port 2E8h-2EFh (COM4) as an LPC Access 0: Disable 1: Enable
2	DP2E	R/W	Enable/Disable Decode Port 238h-23Fh as an LPC Access

			0: Disable 1: Enable
1	DP1E	R/W	Enable/Disable Decode Port 228h-22Fh as an LPC Access 0: Disable 1: Enable
0	DP0E	R/W	Enable/Disable Decode Port 220h-227h as an LPC Access 0: Disable 1: Enable

Register Offset: 53h
Register Name: Internal UART Control Register
Reset Value: 00h

7	6	5	4	3	2	1	0
UIADE	Reserved			UIRT			

Bit	Name	Attribute	Description
7	UIADE	R/W	Enable/Disable Internal UART IO Address Decode 0: Disable 1: Enable
6-4	Rsvd	RO	Reserved
3-0	UIRT	R/W	UART IRQ Routing Table Bit 3 Bit 2 Bit 1 Bit 0 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15] These four bits are used to route UART IRQ to any 8259 Interrupt lines. The BIOS should be used to inhibit the setting of the reserved value.

Register Offset: 57h – 54h
Register Name: Internal UART IO Address Register
Reset Value: 03F8h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UIOA																													Reserved		

Bit	Name	Attribute	Description
31-3	UIOA	R/W	Internal UART IO Address. The Bit[31:3] contain the base IO address A[31:3] of internal UART.
2-0	Rsvd	RO	Reserved. All are '0's. To write any value to these bits causes no effect.

Register Offset: 5Bh – 58h
Register Name: PCI Interrupt Routing Table Register
Reset Value: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EHCIH				OHCIH				MAC1				MAC0				RT3				RT2				RT1				RT0			

Bit	Name	Attribute	Description
31-28	EHCIH	R/W	USB20 EHCI Host Interrupt Routing Table. Bit 31 Bit 30 Bit 29 Bit 28 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
27-24	OHCII	R/W	USB1.1 OHCI interrupt Routing Table. Bit 27 Bit 26 Bit 25 Bit 24 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved

			1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
23-20	MAC1	R/W	MAC1 interrupt Routing Table. Bit 23 Bit 22 Bit 21 Bit 20 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
19-16	MAC0	R/W	MAC0 Interrupt Routing Table. Bit 19 Bit 18 Bit 17 Bit 16 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
15-12	RT3	R/W	INTD_n Routing Table. Bit 15 Bit 14 Bit 13 Bit 12 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
11-8	RT2	R/W	INTC_n Routing Table. Bit 11 Bit 10 Bit 9 Bit 8 Routing Table 0 0 0 0 Disable.

			0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
7-4	RT1	R/W	INTB_n Routing Table. Bit 7 Bit 6 Bit 5 Bit 4 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]
3-0	RT0	R/W	INTA_n Routing Table. Bit 3 Bit 2 Bit 1 Bit 0 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]

Register Offset: 5Fh – 5Ch

Register Name: Buffer Strength Control Register I

Reset Value: 00002EEEh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																DC3		Rsvd	SR3	DC2			SR2	DC1		Rsvd	SR1	DC0			SR0

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved
15-14	DC3	R/W	Output Driving Capability of the ROMCS_n Pin. These three bits are used to select the output driving capability of the ROMCS_n pin. Bit 15 Bit 14 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
13	Rsvd	RO	Reserved
12	SR3	R/W	Output Slew Rate Control of the ROMCS_n Pin. This bit is used to select the output slew rate of the ROMCS_n pin. 0: Fast Slew Rate 1: Slow Slew Rate
11-9	DC2	R/W	Output Driving Capability of the SDRAM Control Signal Output Pins. These three bits are used to select the output driving capability of the SDRAM control signal output pins which include CKE, CS_n, SRAS_n, SCAS_n, SDRAMclk, and WE_n. Bit 11 Bit 10 Bit 9 Driving Current 0 0 0 2 mA 0 0 1 4 mA 0 1 0 6 mA 0 1 1 8 mA 1 0 0 10 mA 1 0 1 12 mA 1 1 0 14 mA 1 1 1 16 mA
8	SR2	R/W	Output Slew Rate Control of the SDRAM Control Signal Output Pins. This bit is used to select the output slew rate of the SDRAM control signal output pins which include CKE, CS_n, SRAS_n, SCAS_n, and WE_n. 0: Fast Slew Rate 1: Slow Slew Rate
7-6	DC1	R/W	Output Driving Capability of the SDRAM MA[12:0] and BA[1:0] Pins. These three bits are used to select the output driving capability of the SDRAM MA[12:0] and BA[1:0] pins. Bit 7 Bit 6 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
5	Rsvd	RO	Reserved
4	SR1	R/W	Output Slew Rate Control of the SDRAM MA[12:0] and BA[1:0] Pins. This bit is used to select the output slew rate for the SDRAM MA[12:0] and BA[1:0] pins. 0: Fast Slew Rate 1: Slow Slew Rate
3-1	DC0	R/W	Output Driving Capability of the SDRAM MD[31:0] and DQM[3:0] Pins. These three bits are used to select the output driving capability of the SDRAM MD[31:0] and DQM[3:0] pins. Bit 3 Bit 2 Bit 1 Driving Current (DQM[3:0]) Driving Current (MD[31:0]) 0 0 0 2 mA 4mA 0 0 1 4 mA 4mA 0 1 0 6 mA 8mA 0 1 1 8 mA 8mA 1 0 0 10 mA 12mA 1 0 1 12 mA 12mA

			1 1 0 1 1 1	14 mA 16 mA	16mA 16mA
0	SR0	R/W	Output Slew Rate Control of the SDRAM MD[31:0] and DQM[3:0] Pins. This bit is used to select the output slew rate of the SDRAM MD[31:0] and DQM[3:0] pins. 0: Fast Slew Rate 1: Slow Slew Rate		

Register Offset: 63h – 60h
Register Name: Buffer Strength Control Register II
Reset Value: 44444443h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												DC0		Rsvd	SR0

Bit	Name	Attribute	Description
31-4	Rsvd	RO	Reserved
3-2	DC0	R/W	Output Driving Capability of the SOUT/GPIO8 and SIN/GPIO7 Pin. These three bits are used to select the output driving capability of the SOUT/GPIO8 and SIN/GPIO7 pin. Bit 3 Bit 2 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
1	Rsvd	RO	Reserved
0	SR0	R/W	Output Slew Rate Control of the SOUT/GPIO8 and SIN/GPIO7 Pin. This bit is used to select the output slew rate of the SOUT/GPIO8 and SIN/GPIO7 pin. 0: Fast Slew Rate 1: Slow Slew Rate

Register Offset: 67h – 64h
Register Name: Buffer Strength Control Register III
Reset Value: 33333333h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC7		Rsvd	SR7	DC6		Rsvd	SR6	DC5		Rsvd	SR5	DC4		Rsvd	SR4	DC3		Rsvd	SR3	DC2		Rsvd	SR2	DC1		Rsvd	SR1	DC0		Rsvd	SR0

Bit	Name	Attribute	Description
31-30	DC7	R/W	Output Driving Capability of the RTS_n/TDO/GPIO9 Pin. These three bits are used to select the output driving capability of the RTS_n/TDO/GPIO9 pin. Bit 31 Bit 30 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
29	Rsvd	RO	Reserved
28	SR7	R/W	Output Slew Rate Control of the RTS_n/TDO/GPIO9 Pin. This bit is used to select the output slew rate of the RTS_n/TDO/GPIO9 Pin. 0: Fast Slew Rate 1: Slow Slew Rate

27-26	DC6	R/W	Output Driving Capability of the DTR_n/GPIO10 Pin. These three bits are used to select the output driving capability of the DTR_n/GPIO10 pin. Bit 27 Bit 26 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
25	Rsvd	RO	Reserved
24	SR6	R/W	Output Slew Rate Control of the DTR_n/GPIO10 Pin. This bit is used to select the output slew rate of the DTR_n/GPIO10 pin. 0: Fast Slew Rate 1: Slow Slew Rate
23-22	DC5	R/W	Output Driving Capability of the CTS_n/TMS/GPIO11 Pin. These three bits are used to select the output driving capability of the CTS_n/TMS/GPIO11 pin. Bit 23 Bit 22 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
21	Rsvd	RO	Reserved
20	SR5	R/W	Output Slew Rate Control of the CTS_n/TMS/GPIO11 Pin. This bit is used to select the output slew rate of the CTS_n/TMS/GPIO11 pin. 0: Fast Slew Rate 1: Slow Slew Rate
19-18	DC4	R/W	Output Driving Capability of the DSR_n/TCK/GPIO12 Pin. These three bits are used to select the output driving capability of the DSR_n/TCK/GPIO12 pin. Bit 19 Bit 18 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
17	Rsvd	RO	Reserved
16	SR4	R/W	Output Slew Rate Control of the DSR_n/TCK/GPIO12 Pin. This bit is used to select the output slew rate of the DSR_n/TCK/GPIO12 pin. 0: Fast Slew Rate 1: Slow Slew Rate
15-14	DC3	R/W	Output Driving Capability of the DCD_n/TDI/GPIO13 Pin. These three bits are used to select the output driving capability of the DCD_n/TDI/GPIO13 pin. Bit 15 Bit 14 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
13	Rsvd	RO	Reserved
12	SR3	R/W	Output Slew Rate Control of the DCD_n/TDI/GPIO13 Pin. This bit is used to select the output slew rate of the DCD_n/TDI/GPIO13 pin. 0: Fast Slew Rate 1: Slow Slew Rate
11-10	DC2	R/W	Output Driving Capability of the RI_n/GPIO14 Pin. These three bits are used to select the output driving capability of the RI_n/GPIO14 pin. Bit 11 Bit 10 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
9	Rsvd	RO	Reserved
8	SR2	R/W	Output Slew Rate Control of the RI_n/GPIO14 Pin. This bit is used to select the output slew rate of the RI_n/GPIO14 pin.

			0: Fast Slew Rate 1: Slow Slew Rate
7-6	DC1	R/W	Output Driving Capability of the RTCAS/GPIO15 Pin. These three bits are used to select the output driving capability of the RTCAS/GPIO15 pin. Bit 7 Bit 6 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
5	Rsvd	RO	Reserved
4	SR1	R/W	Output Slew Rate Control of the RTCAS/GPIO15 Pin. This bit is used to select the output slew rate of the RTCAS/GPIO15 pin. 0: Fast Slew Rate 1: Slow Slew Rate
3-2	DC0	R/W	Output Driving Capability of the RTCRD/GPIO16 Pin. These three bits are used to select the output driving capability of the RTCRD/GPIO16 pin. Bit 3 Bit 2 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
1	Rsvd	RO	Reserved
0	SR0	R/W	Output Slew Rate Control of the RTCRD/GPIO16 Pin. This bit is used to select the output slew rate of the RTCRD/GPIO16 pin. 0: Fast Slew Rate 1: Slow Slew Rate

Register Offset: 6Bh – 68h

Register Name: Buffer Strength Control Register IV

Reset Value: 33333323h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC7		Rsvd	SR7		DC6		Rsvd	SR6		DC5		Rsvd	SR5		Reserved																

Bit	Name	Attribute	Description
31-30	DC7	R/W	Output Driving Capability of the RTCWR/GPIO17 Pin. These three bits are used to select the output driving capability of the RTCWR/GPIO17 pin. Bit 31 Bit 30 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
29	Rsvd	RO	Reserved
28	SR7	R/W	Output Slew Rate Control of the RTCWR/GPIO17 Pin. This bit is used to select the output slew rate of the RTCWR/GPIO17 pin. 0: Fast Slew Rate 1: Slow Slew Rate
27-26	DC6	R/W	Output Driving Capability of the IRQ8_n/GPIO18 Pin. These three bits are used to select the output driving capability of the IRQ8_n/GPIO18 pin. Bit 27 Bit 26 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA

25	Rsvd	RO	Reserved
24	SR6	R/W	Output Slew Rate Control of the IRQ8_n/GPIO18 Pin. This bit is used to select the output slew rate of the IRQ8_n/GPIO18 pin. 0: Fast Slew Rate 1: Slow Slew Rate
23-22	DC5	R/W	Output Driving Capability of the SPKR/GPIO19 Pin. These three bits are used to select the output driving capability of the SPKR/GPIO19 pin. Bit 23 Bit 22 Driving Current 0 0 4 mA 0 1 8 mA 1 0 12 mA 1 1 16 mA
21	Rsvd	RO	Reserved
20	SR5	R/W	Output Slew Rate Control of the SPKR/GPIO19 Pin. This bit is used to select the output slew rate of the SPKR/GPIO19 pin. 0: Fast Slew Rate 1: Slow Slew Rate
19-0	Rsvd	RO	Reserved

Register Offset: 87h – 84h

Register Name: General-Purpose I/O Control Register II

Reset Value: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					G58E	G57E	G56E	G55E	G54E	G53E	G52E	G51E	G50E	G49E	G48E	G47E	G46E	G45E	G44E	G43E	G42E	G41E	G40E	G39E	G38E	G37E	G36E	G35E	G34E	G33E	G32E

Bit	Name	Attribute	Description
31-27	Rsvd	RO	Reserved
26	G58E	R/W	GPIO58 Function Enable/Disable. 0: Disable. This pin operates in normal (CS2_n/CLKIN14.318) function. 1: Enable. This pin operates as GPIO58 with an internal 75KΩ pull-up resistor.
25	G57E	R/W	GPIO57 Function Enable/Disable. 0: Disable. This pin operates in normal (CS1_n) function. 1: Enable. This pin operates as GPIO57 with an internal 75KΩ pull-up resistor.
24	G56E	R/W	GPIO56 Function Enable/Disable. 0: Disable. This pin operates in normal (CLK25MOUT) function. 1: Enable. This pin operates as GPIO56 with an internal 75KΩ pull-up resistor.
23	G55E	R/W	GPIO55 Function Enable/Disable. 0: Disable. This pin operates in normal (KBRST_n) function. 1: Enable. This pin operates as GPIO55 with an internal 75KΩ pull-up resistor.
22	G54E	R/W	GPIO54 Function Enable/Disable. 0: Disable. This pin operates in normal (A20GATE_n) function. 1: Enable. This pin operates as GPIO54 with an internal 75KΩ pull-up resistor.
21	G53E	R/W	GPIO53 Function Enable/Disable. 0: Disable. This pin operates in normal (SPEAKER) function. 1: Enable. This pin operates as GPIO53 with an internal 75KΩ pull-up resistor.
20	G52E	R/W	GPIO52 Function Enable/Disable. 0: Disable. This pin operates in normal (COL0) function. 1: Enable. This pin operates as GPIO52 with an internal 75KΩ pull-up resistor.
19	G51E	R/W	GPIO51 Function Enable/Disable. 0: Disable. This pin operates in normal (RXD0_3) function. 1: Enable. This pin operates as GPIO51 with an internal 75KΩ pull-up resistor.

18	G50E	R/W	GPIO50 Function Enable/Disable. 0: Disable. This pin operates in normal (RXD0_2) function. 1: Enable. This pin operates as GPIO50 with an internal 75KΩ pull-up resistor.
17	G49E	R/W	GPIO49 Function Enable/Disable. 0: Disable. This pin operates in normal (RXD0_1) function. 1: Enable. This pin operates as GPIO49 with an internal 75KΩ pull-up resistor.
16	G48E	R/W	GPIO48 Function Enable/Disable. 0: Disable. This pin operates in normal (RXD0_0) function. 1: Enable. This pin operates as GPIO48 with an internal 75KΩ pull-up resistor.
15	G47E	R/W	GPIO47 Function Enable/Disable. 0: Disable. This pin operates in normal (RXDV0) function. 1: Enable. This pin operates as GPIO47 with an internal 75KΩ pull-up resistor.
14	G46E	R/W	GPIO46 Function Enable/Disable. 0: Disable. This pin operates in normal (RXC0) function. 1: Enable. This pin operates as GPIO46 with an internal 75KΩ pull-up resistor.
13	G45E	R/W	GPIO45 Function Enable/Disable. 0: Disable. This pin operates in normal (TXEN0) function. 1: Enable. This pin operates as GPIO45 with an internal 75KΩ pull-up resistor.
12	G44E	R/W	GPIO44 Function Enable/Disable. 0: Disable. This pin operates in normal (TXD0_3) function. 1: Enable. This pin operates as GPIO44 with an internal 75KΩ pull-up resistor.
11	G43E	R/W	GPIO43 Function Enable/Disable. 0: Disable. This pin operates in normal (TXD0_2) function. 1: Enable. This pin operates as GPIO43 with an internal 75KΩ pull-up resistor.
10	G42E	R/W	GPIO42 Function Enable/Disable. 0: Disable. This pin operates in normal (TXD0_1) function. 1: Enable. This pin operates as GPIO42 with an internal 75KΩ pull-up resistor.
9	G41E	R/W	GPIO41 Function Enable/Disable. 0: Disable. This pin operates in normal (TXD0_0) function. 1: Enable. This pin operates as GPIO41 with an internal 75KΩ pull-up resistor.
8	G40E	R/W	GPIO40 Function Enable/Disable. 0: Disable. This pin operates in normal (TXC0) function. 1: Enable. This pin operates as GPIO40 with an internal 75KΩ pull-up resistor.
7	G39E	R/W	GPIO39 Function Enable/Disable. 0: Disable. This pin operates in normal (SA23) function. 1: Enable. This pin operates as GPIO39 with an internal 75KΩ pull-up resistor.
6	G38E	R/W	GPIO38 Function Enable/Disable. 0: Disable. This pin operates in normal (SA22) function. 1: Enable. This pin operates as GPIO38 with an internal 75KΩ pull-up resistor.
5	G37E	R/W	GPIO37 Function Enable/Disable. 0: Disable. This pin operates in normal (SA21) function. 1: Enable. This pin operates as GPIO37 with an internal 75KΩ pull-up resistor.
4	G36E	R/W	GPIO36 Function Enable/Disable. 0: Disable. This pin operates in normal (SA20) function. 1: Enable. This pin operates as GPIO36 with an internal 75KΩ pull-up resistor.
3	G35E	R/W	GPIO35 Function Enable/Disable. 0: Disable. This pin operates in normal (SA19) function. 1: Enable. This pin operates as GPIO35 with an internal 75KΩ pull-up resistor.
2	G34E	R/W	GPIO34 Function Enable/Disable. 0: Disable. This pin operates in normal (SA18) function. 1: Enable. This pin operates as GPIO34 with an internal 75KΩ pull-up resistor.
1	G33E	R/W	GPIO33 Function Enable/Disable. 0: Disable. This pin operates in normal (SA17) function. 1: Enable. This pin operates as GPIO33 with an internal 75KΩ pull-up resistor.
0	G32E	R/W	GPIO32 Function Enable/Disable. 0: Disable. This pin operates in normal (SA16) function. 1: Enable. This pin operates as GPIO32 with an internal 75KΩ pull-up resistor.

Register Offset: 8Bh – 88h

Register Name: General-Purpose I/O Data Register II

Reset Value: FFFFFFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					G58D	G57D	G56D	G55D	G54D	G53D	G52D	G51D	G50D	G49D	G48D	G47D	G46D	G45D	G44D	G43D	G42D	G41D	G40D	G39D	G38D	G37D	G36D	G35D	G34D	G33D	G32D

Bit	Name	Attribute	Description
31-27	Rsvd	RO	Reserved
26	G58D	R/W	GPIO58 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO58 pin to ‘Low’. Write ‘1’ to this bit to drive theGPIO58 pin to ‘High’. In Input Mode: Read input data of GPIO58 from this bit. ‘1’ means that the external device drives the GPIO58 pin to ‘High’, and ‘0’ means that the external device drives GPIO58 to ‘Low’. A ‘1’ must be written to this bit when GPIO58 is in Input Mode.
25	G57D	R/W	GPIO57 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO57 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO57 pin to ‘High’. In Input Mode: Read input data of GPIO57 from this bit. ‘1’ means that the external device drives the GPIO57 pin to ‘High’, and ‘0’ means that the external device drives GPIO57 to ‘Low’. A ‘1’ must be written to this bit when GPIO57 is in Input Mode.
24	G56D	R/W	GPIO56 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO56 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO56 pin to ‘High’. In Input Mode: Read input data of GPIO56 from this bit. ‘1’ means that the external device drives the GPIO56 pin to ‘High’, and ‘0’ means that the external device drives GPIO56 to ‘Low’. A ‘1’ must be written to this bit when GPIO56 is in Input Mode.
23	G55D	R/W	GPIO55 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO55 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO55 pin to ‘High’. In Input Mode: Read input data of GPIO55 from this bit. ‘1’ means that the external device drives the GPIO55 pin to ‘High’, and ‘0’ means that the external device drives GPIO55 to ‘Low’. A ‘1’ must be written to this bit when GPIO55 is in Input Mode.
22	G54D	R/W	GPIO54 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO54 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO54 pin to ‘High’. In Input Mode: Read input data of GPIO54 from this bit. ‘1’ means that the external device drives the GPIO54 pin to ‘High’, and ‘0’ means that the external device drives GPIO54 to ‘Low’. A ‘1’ must be written to this bit when GPIO54 is in Input Mode.
21	G53D	R/W	GPIO53 Control/Data In Output Mode: Write ‘0’ to this bit to drive the GPIO53 pin to ‘Low’. Write ‘1’ to this bit to drive the GPIO53 pin to ‘High’. In Input Mode: Read input data of GPIO53 from this bit. ‘1’ means that the external device drives the GPIO53 pin to ‘High’, and ‘0’ means that the external device drives GPIO53 to ‘Low’. A ‘1’ must be written to this bit when GPIO53 is in Input Mode.

20	G52D	R/W	GPIO52 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO52 pin to 'Low'. Write '1' to this bit to drive the GPIO52 pin to 'High'. In Input Mode: Read input data of GPIO52 from this bit. '1' means that the external device drives the GPIO52 pin to 'High', and '0' means that the external device drives GPIO52 to 'Low'. A '1' must be written to this bit when GPIO52 is in Input Mode.
19	G51D	R/W	GPIO51 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO51 pin to 'Low'. Write '1' to this bit to drive the GPIO51 pin to 'High'. In Input Mode: Read input data of GPIO51 from this bit. '1' means that the external device drives the GPIO51 pin to 'High', and '0' means that the external device drives GPIO51 to 'Low'. A '1' must be written to this bit when GPIO51 is in Input Mode.
18	G50D	R/W	GPIO50 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO50 pin to 'Low'. Write '1' to this bit to drive theGPIO50 pin to 'High'. In Input Mode: Read input data of GPIO50 from this bit. '1' means that the external device drives the GPIO50 pin to 'High', and '0' means that the external device drives GPIO50 to 'Low'. A '1' must be written to this bit when GPIO50 is in Input Mode.
17	G49D	R/W	GPIO49 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO49 pin to 'Low'. Write '1' to this bit to drive the GPIO49 pin to 'High'. In Input Mode: Read input data of GPIO49 from this bit. '1' means that the external device drives the GPIO49 pin to 'High', and '0' means that the external device drives GPIO49 to 'Low'. A '1' must be written to this bit when GPIO49 is in Input Mode.
16	G48D	R/W	GPIO48 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO48 pin to 'Low'. Write '1' to this bit to drive the GPIO48 pin to 'High'. In Input Mode: Read input data of GPIO48 from this bit. '1' means that the external device drives the GPIO48 pin to 'High', and '0' means that the external device drives GPIO48 to 'Low'. A '1' must be written to this bit when GPIO48 is in Input Mode.
15	G47D	R/W	GPIO47 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO47 pin to 'Low'. Write '1' to this bit to drive the GPIO47 pin to 'High'. In Input Mode: Read input data of GPIO47 from this bit. '1' means that the external device drives the GPIO47 pin to 'High', and '0' means that the external device drives GPIO47 to 'Low'. A '1' must be written to this bit when GPIO47 is in Input Mode.
14	G46D	R/W	GPIO46 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO46 pin to 'Low'. Write '1' to this bit to drive the GPIO46 pin to 'High'. In Input Mode: Read input data of GPIO46 from this bit. '1' means that the external device drives the GPIO46 pin to 'High', and '0' means that the external device drives GPIO46 to 'Low'. A '1' must be written to this bit when GPIO46 is in Input Mode.
13	G45D	R/W	GPIO45 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO45 pin to 'Low'. Write '1' to this bit to drive the GPIO45 pin to 'High'. In Input Mode:

			Read input data of GPIO45 from this bit. '1' means that the external device drives the GPIO45 pin to 'High', and '0' means that the external device drives GPIO45 to 'Low'. A '1' must be written to this bit when GPIO45 is in Input Mode.
12	G44D	R/W	GPIO44 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO44 pin to 'Low'. Write '1' to this bit to drive the GPIO44 pin to 'High'. In Input Mode: Read input data of GPIO44 from this bit. '1' means that the external device drives the GPIO44 pin to 'High', and '0' means that the external device drives GPIO44 to 'Low'. A '1' must be written to this bit when GPIO44 is in Input Mode.
11	G43D	R/W	GPIO43 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO43 pin to 'Low'. Write '1' to this bit to drive the GPIO43 pin to 'High'. In Input Mode: Read input data of GPIO43 from this bit. '1' means that the external device drives the GPIO43 pin to 'High', and '0' means that the external device drives GPIO43 to 'Low'. A '1' must be written to this bit when GPIO43 is in Input Mode.
10	G42D	R/W	GPIO42 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO42 pin to 'Low'. Write '1' to this bit to drive the GPIO42 pin to 'High'. In Input Mode: Read input data of GPIO42 from this bit. '1' means that the external device drives the GPIO42 pin to 'High', and '0' means that the external device drives GPIO42 to 'Low'. A '1' must be written to this bit when GPIO42 is in Input Mode.
9	G41D	R/W	GPIO41 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO41 pin to 'Low'. Write '1' to this bit to drive the GPIO41 pin to 'High'. In Input Mode: Read input data of GPIO41 from this bit. '1' means that the external device drives the GPIO41 pin to 'High', and '0' means that the external device drives GPIO41 to 'Low'. A '1' must be written to this bit when GPIO41 is in Input Mode.
8	G40D	R/W	GPIO40 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO40 pin to 'Low'. Write '1' to this bit to drive the GPIO40 pin to 'High'. In Input Mode: Read input data of GPIO40 from this bit. '1' means that the external device drives the GPIO40 pin to 'High', and '0' means that the external device drives GPIO40 to 'Low'. A '1' must be written to this bit when GPIO40 is in Input Mode.
7	G39D	R/W	GPIO39 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO39 pin to 'Low'. Write '1' to this bit to drive the GPIO39 pin to 'High'. In Input Mode: Read input data of GPIO39 from this bit. '1' means that the external device drives the GPIO39 pin to 'High', and '0' means that the external device drives GPIO39 to 'Low'. A '1' must be written to this bit when GPIO39 is in Input Mode.
6	G38D	R/W	GPIO38 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO38 pin to 'Low'. Write '1' to this bit to drive the GPIO38 pin to 'High'. In Input Mode: Read input data of GPIO38 from this bit. '1' means that the external device drives the GPIO38 pin to 'High', and '0' means that the external device drives GPIO38 to 'Low'. A '1' must be written to this bit when GPIO38 is in Input Mode.
5	G37D	R/W	GPIO37 Control/Data In Output Mode:

			Write '0' to this bit to drive the GPIO37 pin to 'Low'. Write '1' to this bit to drive the GPIO37 pin to 'High'. In Input Mode: Read input data of GPIO37 from this bit. '1' means that the external device drives the GPIO37 pin to 'High', and '0' means that the external device drives GPIO37 to 'Low'. A '1' must be written to this bit when GPIO37 is in Input Mode.
4	G36D	R/W	GPIO36 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO36 pin to 'Low'. Write '1' to this bit to drive the GPIO36 pin to 'High'. In Input Mode: Read input data of GPIO36 from this bit. '1' means that the external device drives the GPIO36 pin to 'High', and '0' means that the external device drives GPIO36 to 'Low'. A '1' must be written to this bit when GPIO36 is in Input Mode.
3	G35D	R/W	GPIO35 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO35 pin to 'Low'. Write '1' to this bit to drive the GPIO35 pin to 'High'. In Input Mode: Read input data of GPIO35 from this bit. '1' means that the external device drives the GPIO35 pin to 'High', and '0' means that the external device drives GPIO35 to 'Low'. A '1' must be written to this bit when GPIO35 is in Input Mode.
2	G34D	R/W	GPIO34 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO34 pin to 'Low'. Write '1' to this bit to drive the GPIO34 pin to 'High'. In Input Mode: Read input data of GPIO34 from this bit. '1' means that the external device drives the GPIO34 pin to 'High', and '0' means that the external device drives GPIO34 to 'Low'. A '1' must be written to this bit when GPIO34 is in Input Mode.
1	G33D	R/W	GPIO33 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO33 pin to 'Low'. Write '1' to this bit to drive the GPIO33 pin to 'High'. In Input Mode: Read input data of GPIO33 from this bit. '1' means that the external device drives the GPIO33 pin to 'High', and '0' means that the external device drives GPIO33 to 'Low'. A '1' must be written to this bit when GPIO33 is in Input Mode.
0	G32D	R/W	GPIO32 Control/Data In Output Mode: Write '0' to this bit to drive the GPIO32 pin to 'Low'. Write '1' to this bit to drive the GPIO32 pin to 'High'. In Input Mode: Read input data of GPIO32 from this bit. '1' means that the external device drives the GPIO32 pin to 'High', and '0' means that the external device drives GPIO32 to 'Low'. A '1' must be written to this bit when GPIO32 is in Input Mode.

Register Offset: 93h – 90h

Register Name: Chip Select 1 Base Address Register

Reset Value: 00321007h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address																								Reserved					Bit16	MIO	En

Bit	Name	Attribute	Description

31-8	BA	R/W	Chip Select 1 Base Address A[31:8]. I/O map only uses A[15:8]; others are reserved. Chip Select 1 starts at the base address.
7-3	Rsvd	R	Reserved
2	BIT16	R/W	0: 8-bit 1: 16-bit
1	MIO	R/W	0: I/O map 1: Memory maps I/O
0	En	R/W	Chip Select 1 Base Address is enabled when set

Register Offset: 97h – 94h
Register Name: Chip Select 1 Base Address Mask
Reset Value: FFFFFF00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAM																								Reserved							

Bit	Name	Attribute	Description
31-8	BAM	R/W	Chip Select 1 Base Address Mask bit [31:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 9Bh – 98h
Register Name: Chip Select 2 Base Address Register
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address																								Reserved					Bit16	MIO	En

Bit	Name	Attribute	Description
31-8	BA	R/W	Chip Select 2 Base Address A[31:8]. I/O map only uses A[15:8]; others are reserved. Chip Select 2 starts at the base address.
7-3	Rsvd	R	Reserved
2	BIT16	R/W	0: 8-bit 1: 16-bit
1	MIO	R/W	0: I/O map 1: Memory maps I/O
0	En	R/W	Chip Select 2 Base Address is enabled when set

Register Offset: 9Fh – 9Ch
Register Name: Chip Select 2 Base Address Mask
Reset Value: FFFFFF00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

BAM	Reserved

Bit	Name	Attribute	Description
31-8	BAM	R/W	Chip Select 2 Base Address Mask bit [31:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

11.3.3 MAC1 and MAC2 Configuration Registers

Register Offset: 01h – 00h
Register Name: Vendor ID Register
Reset Value: 17F3h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
17F3h															

Bit	Name	Attribute	Description
15-0	VID	RO	This register contains a 16-bit value assigned to RDC Semiconductor Co., Ltd.

Register Offset: 03h – 02h
Register Name: Device ID Register
Reset Value: 6040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6040h															

Bit	Name	Attribute	Description
15-0	DID	RO	This register contains a 16-bit value to specify a particular device.

Register Offset: 05h – 04h
Register Name: Command Register
Reset Value: 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													PMDC	MSAC	IOSAC

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved. These bits always return ’0’s.
2	PMDC	R/W	PCI Bus Master Device Control. This bit always returns ‘1’.

1	MSAC	R/W	Memory Space Access Control. This bit always returns ‘1’.
0	IOSAC	R/W	I/O Space Access Control. This bit always returns ‘1’.

Register Offset: 07h – 06h
Register Name: Status Register
Reset Value: 0200h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	SS	RMAS	RTAS	STAS	DT		Reserved								

Bit	Name	Attribute	Description
15	DPE	RO	Detected Parity Error. This bit must be set whenever the device detects a parity error. This is a read-only bit and is cleared by writing '1' to it.
14	SS	RO	SERR_n Status. This bit must be set whenever the device asserts SERR_n. This is a read-only bit and is cleared by writing '1' to it.
13	RMAS	RO	Receive Master Abort Status when the MAC acts as a master. This bit is set to '1' when the R3210 generates a transaction (except for special cycles), and is terminated with master-abort. This is a read-only bit and is cleared by writing '1' to it.
12	RTAS	RO	Receive Target Abort Status when the MAC acts as a master. This bit is set to '1' when the MAC encounters a target abort condition. This is a read-only bit and is cleared by writing a '1' to it.
11	STAS	RO	Signal Target Abort Status when the MAC acts as a slave. The R6040 as a slave never generates a Target abort. This bit is always 0.
10-9	DT	RO	DEVSEL_n Timing. The MAC always generates DEVSEL_n with low timing. These bits are always ‘10’.
8-0	Rsvd	RO	Reserved. These bits always return ’0’s.

Register Offset: 08h
Register Name: Revision ID Register
Reset Value: 00h

7	6	5	4	3	2	1	0
RID							

Bit	Name	Attribute	Description
7-0	RID	R/W	Version number of the R6040 MAC

Register Offset: 0Bh – 09h
Register Name: Class Code Register
Reset Value: 020000h

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC																							

Bit	Name	Attribute	Description
23-0	CC	RO	Class Code of the R6040 FastEthernet Controller.

Register Offset: 0Eh
Register Name: Header Type Register
Reset Value: 00h

7	6	5	4	3	2	1	0
HT							

Bit	Name	Attribute	Description
7-0	HT	RO	This register identifies the type of predefined header in the configuration space.

Register Offset: 13h – 10h
Register Name: I/O Base Address Register
Reset Value: XXXXXX01h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAD																								Reserved							1

Bit	Name	Attribute	Description
31-8	BAD	R/W	I/O Base Address.
7-1	Rsvd	RO	Reserved.
0	1	RO	Always 1, I/O space indicator.

Register Offset: 17h – 14h
Register Name: Memory Base Address Register
Reset Value: XXXXXX00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAD																								Reserved							0

Bit	Name	Attribute	Description
31-8	BAD	R/W	Memory Base Address.
7-1	Rsvd	RO	Reserved.
0	0	RO	Always 0, memory space indicator.

Register Offset: 2Dh – 2Ch
Register Name: Subsystem Vendor ID Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVID															

Bit	Name	Attribute	Description
15-0	SVID	R/WL	This register contains the subsystem Vendor ID.

Register Offset: 2Fh – 2Eh
Register Name: Subsystem Device ID Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDID															

Bit	Name	Attribute	Description
15-0	SDID	R/WL	This register contains the subsystem Device ID.

Register Offset: 3Dh – 3Ch
Register Name: Interrupt Control Register
Reset Value: 01XXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTP								INTL							

Bit	Name	Attribute	Description
15-8	INTP	R	Interrupt Pin. Use INT_A.
7-0	INTL	R/W	Interrupt Line. Index Interrupt Vector.

12. USB2.0 Host Controller

12.1 Features

The USB2.0 Host Controller is a two-port host controller which contains one OHCI host controller compliant with OpenHCI standard developed by Compaq, Microsoft and National Semiconductor and one EHCI host controller compliant with EHCI1.0 specification developed by Intel. Features of the USB2.0 host controller are described as below:

12.1.1 USB1.1 Host Controller

- Supports all full-speed (12MHz) and low-speed (1.5MHz) devices compliant with the "USB Specification" version1.0.
- Supports four transfers: control, bulk, interrupt and isochronous transfers.
- Supports up to 127 devices at the same time.
- Contains one 64-byte FIFO.

12.1.2 USB2.0 Host Controller

- Supports all high-speed (480MHz) devices compliant with the "USB Specification" version2.0.
- Supports four transfers: control, bulk, interrupt and isochronous transfers.
- Supports split transaction for USB2.0 Hub plugged with USB1.1 devices.
- Supports up to 127 devices at the same time.
- Contains two 1K-byte FIFO, one for TX and one for RX.

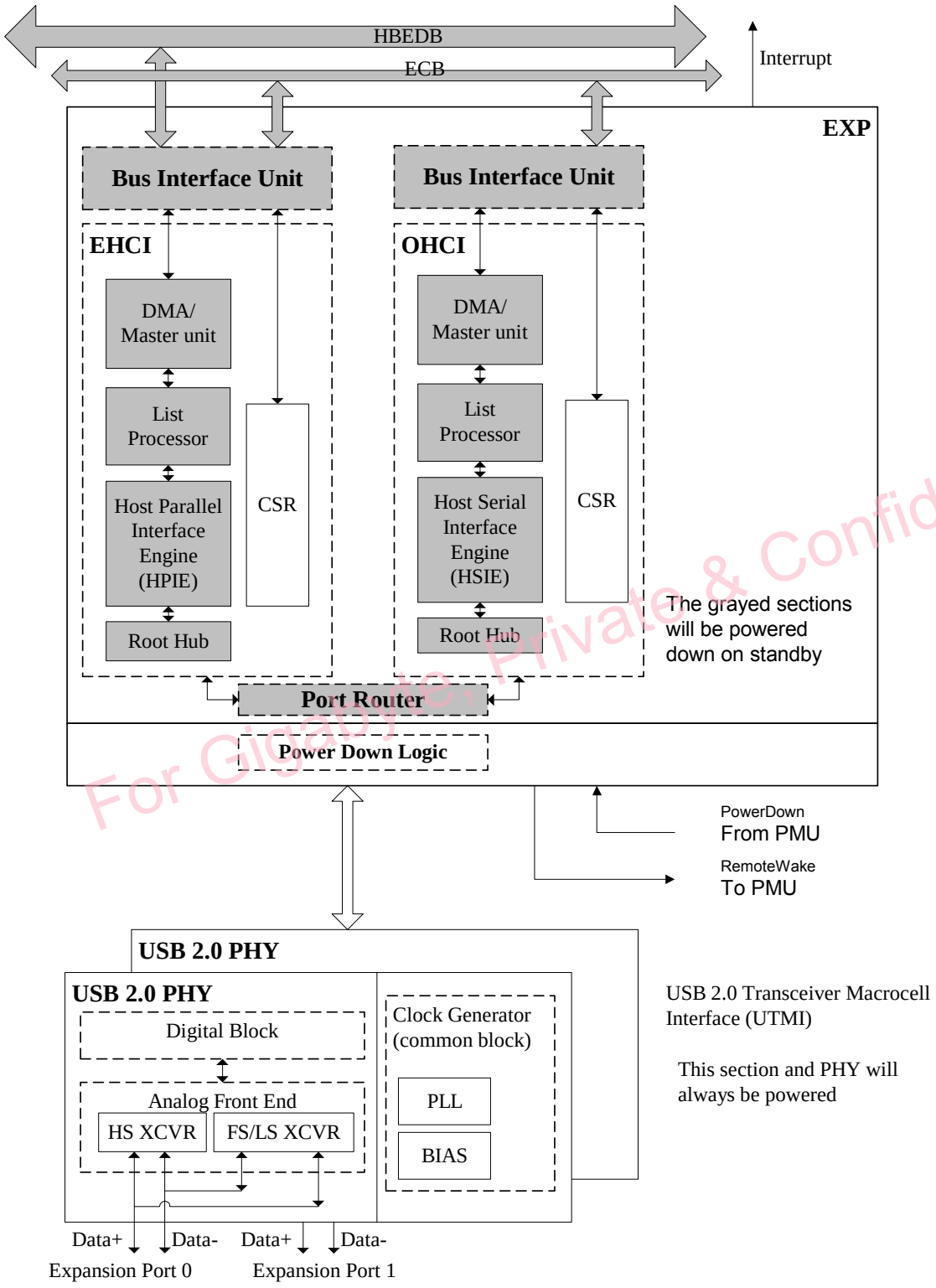
12.2 General Descriptions

The USB 2.0 Host Controller includes one high-speed mode host controller and one USB 1.1 host controller (OHCI). The high-speed host controller implements an EHCI interface. It is used for all high-speed communications to high-speed-mode devices connected to the root ports of the USB 2.0 host controller. It allows communications to full- and low-speed devices connected to the root ports of the USB 2.0 host controller to be provided by the USB 1.1 host controller.

This architecture allows the USB 2.0 host controller to provide USB functionality as long as there is at least USB 1.1 software support in the resident operating system. Full USB 2.0 functionality is delivered when both USB 1.1 and EHCI software is available in the operating system. The port transceiver routing logic is key to delivering this flexible operating environment. The state of the routing logic initially depends on whether software has configured the EHCI controller. Once the EHCD driver has configured the EHCI controller, it can specifically release the transceiver to the companion host controller port register if the attached device is not a high-speed device. When the operating system does not include support for the EHCI controller, the ports are default-routed to the USB1.1 host controllers and the existing USB support for Full- and Low-speed devices remains. The USB1.1 host controllers always manage Full- and Low-speed USB devices connected to the root ports.

High-speed devices are always routed to and controlled by the EHCI host controller (eHC). When running and configured, the eHC is the default *owner* of all the root ports. The eHC and its driver initially detect all devices attached. It has additional control bits visible in each port register to manage the routing logic. For example: if the attached device is not a high-speed device, the eHC driver releases ownership of the port (and thus control the device) to a companion host controller. For that port, enumeration starts over from the initial attached detect point and the device is enumerated under the USB1.1 host controller. Otherwise, the eHC retains ownership of the port and the device completes enumeration under the eHC.

12.3 Functional Block Diagram



12.4 Functional Block Descriptions

12.4.1 DMA/Master Unit

The Bus Master Controller provides the PCI Interface (PCI IF) with the signals necessary to perform PCI cycles on behalf of the Data Buffer Engine (not shown in the block diagram) or List Processor. These signals include the address of the first byte in the transfer, the size of the transfer in bytes, the direction of the transfer, and the data for write cycles. The PCI IF will carry out the appropriate PCI cycle based on the provided information. In addition, there are three control signals across the interface: a request signal from the Bus Master Controller, a cycle active and a data ready signal from the PCI Controller. The Bus Master Controller requests access when it is necessary to transfer a cycle on the PCI Bus. When access is granted, the PCI IF asserts the cycle active signal which remains asserted until the cycle completes. The PCI IF asserts the data ready signal for one PCI period for each Dword transfer across the interface. On a write, the data ready signal indicates that the PCI IF has consumed the Dword presented by the Bus Master Controller. On a read, the data ready signal indicates that a valid Dword is present on the PCI read data bus.

The Bus Master Controller maintains the address of the next PCI cycle to be requested. The address is initialized with a value from the List Processor when it initiates a request. The address is updated after each burst transfer completes. This is necessary for data transfers that require more than a single burst cycle.

12.4.2 List Processor

The List Processor manages the data structures from the Host Controller Driver and coordinates all activities within the Host Controller. The List Processor has three main control sections that operate in a hierarchical fashion.

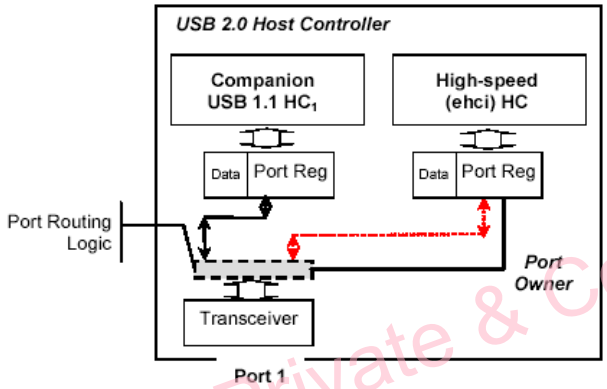
- List Control -- This is at the highest level of the control hierarchy. It schedules which type of list (Isochronous, Interrupt, Bulk or Control) is processed.
- Endpoint Descriptor (Queue Head Descriptor) Control -- This is at the middle level of the control hierarchy. Once the List Control detected a valid list to process, this controls the loading, processing of the Transfer Descriptor, and write-back of the Endpoint Descriptor for the current list.
- Transfer Descriptor (Queue Head Transfer Descriptor, iTD Descriptor, SiTD Descriptor) Control -- This is at the lowest level of the control hierarchy. Once the Endpoint Descriptor (QH) Control loaded a valid ED (QH), this controls the loading, processing of the data transfer, and write-back of the Transfer Descriptor (qTD, …) for the current ED (QH).

12.4.3 Host Parallel Interface Engine (HPIE) or Host Serial Interface Engine (HSIE)

The HPIE is for USB2.0 and the HSIE is for USB1.1.
The HPIE (HSIE) is responsible for managing all transactions to the USB. It controls the bus protocol, packet generation/extraction, data parallel-to-serial conversion, CRC coding, bit stuffing, and NRZI encoding.
All transactions on the USB are requested by the List Processor and Frame Manager (not shown in the block diagram). After the List Processor retrieves all information necessary to initiate communication to a USB device, it generates a request to the HPIE (HSIE) accompanied by endpoint specific control information required to generate proper protocol and packet formats to establish the desired communication pipe. The data buffer provides a data path for the data packets and controls the number of bytes transferred.

12.4.4 Port Router

The USB 2.0 host controller is comprised of one high-speed host controller which implements the EHCI programming interface and one OHCI host controllers. This configuration is used to deliver the required full USB 2.0-defined port capability; e.g. low-, full-, and high-speed capability for every port. The figure shown below illustrates a simple block diagram of the port routing logic and its relationship to the high-speed and OHCI host controllers within a USB 2.0 host controller.



There exists one transceiver per physical port and each host controller module has its own port status and control registers. The EHCI controller has port status and control registers for every port. The OHCI host controller has only the port control and status registers it is required to operate. Each transceiver can be controlled by either the EHCI host controller or the OHCI host controller. Routing logic lies between the transceiver and the port status and control registers. The port routing logic is controlled from signals originating in the EHCI host controller. The EHCI host controller has a *global* routing policy control field and per-port *ownership* control fields. The *Configured Flag* (*CF*) bit (defined in OP register of EHCI) is the global routing policy control. At power-on or reset, the default routing policy is to the companion controllers (if they exist). In general, when the EHCI owns the ports, the companion host controllers' port registers do not see a connect indication from the transceiver. Similarly, when the OHCI host controller owns a port, the EHCI controller's port registers do not see a connect indication from the transceiver.

12.4.5 UTMI

This block handles the low-level USB protocol and signaling. This includes features such as data serialization and de-serialization, bit stuffing and clock recovery and synchronization. The primary focus of this block is to shift the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic in the ASIC.

12.5 Register Definition

12.5.1 USB1.1 Configuration Space

Register Offset: 01h – 00h
Register Name: Vendor ID Register
Reset Value : 17F3h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VID															

Bit	Name	Attribute	Description
15-0	VID	RO	Vendor ID

Register Offset: 03h – 02h
Register Name: Device ID Register
Reset Value : 6060h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID															

Bit	Name	Attribute	Description
15-0	DID	RO	Device ID

Register Offset: 05h – 04h
Register Name: Command Register
Reset Value : 0000h
Recommend Value: 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						BBE	SDE	Reserved			MWIC	SCE	PME	ME	IOE

Bit	Name	Attribute	Description
15-10	Rsvd	R/W	Reserved bits. These bits are always 0. Power on Value: 0. Recommend Setting: 0.
9	BBE	R/W	Back to Back Enable USB HC only acts as a master to a single device, so this functionality is not needed. This bit is always 0. Power on Value: 0b. Recommend Setting: 0b.
8	SDE	R/W	SERR_n (Response) Detection Enable bit If set to 1, USB HC asserts SERR_n when it detects an address parity error. SERR_n is not asserted if this bit is 0. Power on Value: 0b. Recommend Setting: 0b.
7-5	Rsvd	R/W	Reserved bits. These bits are always 0. Power on Value: 0b. Recommend Setting: 0b.
4	MWIC	R/W	Memory Write and Invalidate Command If set to 1, USB HC is enabled to run Memory Write and Invalidate commands. The Memory Write and Invalidate Command will only occur if the cacheline size is set to 32 bytes and the memory write is exactly one cacheline. Power on Value: 0b. Recommend Setting: 0b.
3	SCE	R/W	Special Cycle Enable USB HC does not run special cycles on PCI. This bit is always 0. Power on Value: 0b. Recommend Setting: 0b.
2	PME	R/W	PCI Master Enable If set to 1, USB HC is enabled to run PCI master cycles. Power on Value: 0b. Recommend Setting: 1b.
1	ME	R/W	Memory Enable If set to 1, USB HC is enabled to respond as a target to memory cycles. Power on Value: 0b. Recommend Setting: 1b.
0	IOE	R/W	I/O Enable If set to 1, USB HC is enabled to respond as a target to I/O cycles. Power on Value: 0b. Recommend Setting: 1b.

Register Offset: 07h – 06h
Register Name: Status Register
Reset Value : 0280h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	SS	RMAS	RTAS	STAS	DEVSELT		DPRP	FBBC	Reserved			INTS	Reserved		

Bit	Name	Attribute	Description
15	DPE	R/W	Detected Parity Error This bit is set to 1 whenever USB HC detects a parity error, even if the Parity Error (Response) Detection Enable bit is disabled. Cleared by writing a 1 to it.
14	SS	R/W	SERR_n Status This bit is set to 1 whenever the USB HC detects a PCI address parity error. Cleared by writing a 1 to it.
13	RMAS	R/W	Received Master Abort Status Set to 1 when USB HC, acting as a PCI master, aborts a PCI bus memory cycle. Cleared by writing a 1 to it.
12	RTAS	R/W	Received Target Abort Status This bit is set to 1 when a USB HC generated PCI cycle (USB HC is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.
11	STAS	R/W	Signaled Target Abort Status This bit is set to 1 when USB HC signals target aborts. Cleared by writing a 1 to it.
10-9	DEVSELT	R/W	DEVSEL_n timing Read only bits indicating DEVSEL_n timing when a positive decode is performed. Since DEVSEL_n is asserted to meet the medium timing, these bits are encoded as 01b.
8	DPRP	R/W	Data Parity Reported Set to 1 if the Parity Error Response bit is set, and USB HC detects PERR_n asserted while acting as PCI master (whether PERR_n was driven by USB HC or not).
7	FBBC	R/W	Fast Back-to-Back Capable USB HC does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6-4	Rsvd	R/W	Reserved Bits These bits are always 0.
3	INTS	RO	Interrupt Status This bit reflects the state of interrupts in the device.
2-0	Rsvd	R/W	Reserved Bits These bits are always 0.

Register Offset: 08h
Register Name: Revision ID Register
Reset Value : 07h

7	6	5	4	3	2	1	0
FTRVL							

Bit	Name	Attribute	Description
7-0	FTRVL	RO	Functional Revision Level

Register Offset: 0Bh – 09h
Register Name: Class Code Register
Reset Value : 0C0310h

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCLS								SUBCLS								PRGIF							

Bit	Name	Attribute	Description
23-16	BCLS	RO	Base Class The Base Class is 0Ch (Serial Bus Controller).
15-8	SUBCLS	RO	Sub Class The Sub Class is 03h (Universal Serial Bus).
7-0	PRGIF	RO	Programming Interface The Programming Interface is 10h (OpenHCI).

Register Offset: 0Ch
Register Name: Cache Line Size Register
Reset Value : 00h
Recommend Value: 08h

7	6	5	4	3	2	1	0
CCHLSZ							

Bit	Name	Attribute	Description
7-0	CCHLSZ	R/W	Cache Line Size This register identifies the system cache line size in units of 32-bit words. USB HC will only store the value of bit 3 in this register since the cache line size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

Register Offset: 0Dh
Register Name: Latency Timer Register
Reset Value : 00h
Recommend Value: 20h

7	6	5	4	3	2	1	0
LTCTimer							

Bit	Name	Attribute	Description
7-0	LTCTimer	R/W	Latency Timer This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles.

Register Offset: 0Eh
Register Name: Header Type Register
Reset Value : 80h/00h (function0/function1-3)

7	6	5	4	3	2	1	0
HT							

Bit	Name	Attribute	Description
7-0	HT	RO	Header Type Register This register identifies the type of the predefined header in the configuration space. HC0 bit7 of this register is used to identify a multifunction device. When more than one USB HC is enabled, the read out value for HC0 is 80h, and those for HC1, HC2 and EHCI are 00h.

Register Offset: 13h – 10h
Register Name: Base Address Register
Reset Value : 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAD																				Reserved											

Bit	Name	Attribute	Description
31-12	BAD	R/W	Base Address POST writes the value of the memory base address to this register.
11-0	Rsvd	RO	Always 0. Indicates a 4K-byte address range is requested.

Register Offset: 2Dh – 2Ch
Register Name: Subsystem Vendor ID Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVID															

Bit	Name	Attribute	Description
15-0	SVID	R/WL	This register contains the subsystem Vendor ID.

Register Offset: 2Fh – 2Eh
Register Name: Subsystem Device ID Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDID															

Bit	Name	Attribute	Description
15-0	SDID	R/WL	This register contains the subsystem Device ID.

Register Offset: 3Dh – 3Ch
Register Name: Interrupt Control Register
Reset Value: 01XXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTP								INTL							

Bit	Name	Attribute	Description
15-8	INTP	R	Interrupt Pin. Use INT_A.
7-0	INTL	R/W	Interrupt Line. Index Interrupt Vector.

Register Offset: 3Eh
Register Name: Minimum Grant Register
Reset Value : 00h

7	6	5	4	3	2	1	0
MINGNT							

Bit	Name	Attribute	Description
7-0	MINGNT	RO	Minimum Grant.

Register Offset: 3Fh
Register Name: Max Latency Register
Reset Value : 50h

7	6	5	4	3	2	1	0
MAXLAT							

Bit	Name	Attribute	Description
7-0	MAXLAT	RO	Maximum Latency.

Register Offset: 44h
Register Name: Operational Mode Enable Register I
Reset Value : 2ah
Recommend Value: 5ch

7	6	5	4	3	2	1	0
Rsvd	BUO	NR3HS	H910E	PES	BUFUNDEREOF	S3WU	DBR16

Bit	Name	Attribute	Description
7	Rsvd	R/W	Reserved. Power on Value: 0b. Recommend Setting: 0b.
6	BUO	R/W	Buffer Under Orphan. When set, it will fix the problem happened in DB module. The buffer point will reset while data underrun is occurred. Power on Value: 0b. Recommend Setting: 1b.
5	NR3HS	R/W	NoResp3HS. The bit is low active. When cleared, the Error interrupt is reported after three consecutive USB bus transfer error. Power on Value: 1b. Recommend Setting: 0b.

4	H910E	R/W	HcControl bit 9 and bit10 Function Enable. When this bit is set, the function of RemoteWakeupConnected and RemoteWakeupEnable in OHCI will be enabled. Otherwise, these two bits are always cleared. Power on Value: 0b. Recommend Setting: 1b.
3	PES	R/W	PCI EDB Select. When this bit is set, USB HC selects EDB as DMA channel. Power on Value: 1b. Recommend Setting: 1b.
2	BUFUNDEREOF	R/W	Buffer Under End of Frame. Setting this bit will stop the Data Buffer Module function until next access. Power on Value: 0b. Recommend Setting: 1b.
1	S3WU	R/W	S3 Wakeup. The HC will accept wait-state write command after leaving suspend mode if there are no device attached. Power on Value: 1b. Recommend Setting: 0b.
0	DBR16	R/W	Data Buffer Region 16. When the size of the region set for the data buffer is 16 bytes. Otherwise, the size is 32 bytes. Power on Value: 0b. Recommend Setting: 0b.

Register Offset: 45h

Register Name: Operational Mode Enable Register II

Reset Value : 00h

Recommend Value: ach/aeh (P4 system/K8 system)

7	6	5	4	3	2	1	0
DSCE	Rsvd	SUPO	MP	DRE	RFE	Rsvd	

Bit	Name	Attribute	Description
7	DSCE	R/W	Delay Suspend Clock Enable. When this bit is set, the HC generates 4T 12M clock before entering USB suspend state. Power on Value: 0b. Recommend Setting: 1b.
6	Rsvd	R/W	Reserved. Power on Value: 0b. Recommend Setting: 0b.
5	SUPO	R/W	Set USB Power OK. This bit enables USB IO port to drive bus. When this bit is 0, the HC cannot drive any signals to USB bus. Power on Value: 0b. Recommend Setting: 1b.
4	MP	R/W	Mask PMCS. OpenHCI host controllers optional support power management capability function. When this bit is set, the HC is PCI2.2 compliant. PMCS is masked Power on Value: 0b. Recommend Setting: 0b.
3	DRE	R/W	Drive Resume Enable. When this bit is set, the HC will drive resume signal to downstream port that sent remote wakeup signal in S3 or S4. Power on Value: 0b. Recommend Setting: 1b.

2	RFE	R/W	Restore Function Enable. Setting this bit can automatically restore all OHCI OP register after resuming from S3 or S4. Power on Value: 0b. Recommend Setting: 1b.
1-0	Rsvd	R/W	Reserved. Power on Value: 0b. Recommend Setting: 0b.

Register Offset: 46h
Register Name: Operational Mode Enable Register III
Reset Value : 00h
Recommend Value: 01h

7	6	5	4	3	2	1	0
Reserved							RDRST

Bit	Name	Attribute	Description
7-1	Rsvd	R/W	Reserved
0	RDRST	R/W	Ready for Restore. When this bit is set, the HC automatically restores OP registers after resuming from S3. Power on Value: 0b. Recommend Setting: 1b.

Register Offset: 49h – 48h
Register Name: Operational Mode Enable Register IV (For Power Management)
Reset Value : 00h
Recommend Value: 00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit	Name	Attribute	Description
15-0	Rsvd	R/W	Reserved for Power Management & Debug port. Power on Value: 0b. Recommend Setting: 0b.

12.5.2 USB1.1 Operational Registers

The base address of these registers is programmable by the memory base address register (USB PCI configuration register offset 10h – 13h). These registers should be written as Dword. Bytes write to these registers may have unpredictable effects.

The OpenHCI Host Controller (HC) contains a set of on-chip operational registers that are mapped into a non-cacheable portion of the system addressable space. These registers are used by the Host Controller Driver (HCD). According to the functions of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as Dwords.

Reserved bits may be allocated in future releases of this specification. To ensure interoperability, the Host Controller Driver that does not use a reserved field should not assume that the reserved field contains 0. Furthermore, the Host Controller Driver should always preserve the value(s) of the reserved field. When a R/W register is modified, the Host Controller Driver should first read the register, modify the bits desired, then write the register with the reserved bits still containing the read value. Alternatively, the Host Controller Driver can maintain an in-memory copy of previously written values that can be modified and then written to the Host Controller register. When a write to set/clear register is written, bits written to reserved fields should be 0.

12.5.2.1 Open Host Controller Interface Operational Registers

Offset	Register Name
00h	HC Revision
04h	HC Control
08h	HC Command Status
0Ch	HC Interrupt Status
10h	HC Interrupt Enable
14h	HC Interrupt Disable
18h	HC HCCA
1Ch	HC Period Current ED
20h	HC Control Head ED
24h	HC Control Current ED
28h	HC Bulk Head ED
2Ch	HC Bulk Current ED
30h	HC Done Head
34h	HC Fm Interval
38h	HC Fm Remaining
3Ch	HC Fm Number
40h	HC Periodic Start
44h	HC LS Threshold
48h	HC Rh Descriptor A
4Ch	HC Rh Descriptor B
50h	HC Rh Status
54h	HC Rh Port Status [1]
58h	HC Rh Port Status [2]
5Ch – FFh	Reserved
100h	HC eControl
104h	HC eInput
108h	HC eOutput
10Ch	HC eStatus

12.5.2.2 Control and Status Partition

Register Offset: 00h
Register Name: HC Revision Register
Reset Value : 00000110h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																							LG	RV							

Bit	Name	Attribute	Description
31-9	Rsvd	RO	Reserved.
8	LG	RO	Legacy. This read-only field is 1 to indicate that the legacy support registers are present in this HC.
7-0	RV	RO	Revision. This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 11h corresponds to version 1.1. All of the HC implementations that are compliant with current OpenHCI 1.0 specification will have a value of 10h.

Register Offset: 04h
Register Name: HC Control Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																					RMWUEn	RMWUC	INTRT	HCFSUSB			BLEn	CTLEn	IEn	PLEn	CTBSRT

The HC Control Register defines the operating modes for the Host Controller. Only the Host Controller Driver, except Host Controller Functional State and Remote Wakeup Connected, modifies most of the fields in this register.

Bit	Name	Attribute	Description
31-11	Rsvd	RO	Reserved.
10	RMWUEn	RO	Remote Wakeup Enable. This bit is used by the HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the Resume Detected bit in HC Interrupt Status is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	RMWUC	RO	Remote Wakeup Connected. This bit indicates whether the HC supports remote wakeup signaling or not. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. The HC clears the bit upon a hardware reset but does not alter it upon a software reset.
8	INTRT	R/W	Interrupt Routing. This bit determines the routing of interrupts generated by events registered in HC Interrupt Status. If cleared, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. The HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. The HCD uses this bit as a tag to indicate the ownership of HC.
97-6	HCFSUSB	R/W	Host Controller Functional State for USB. 00b: USB Reset

			01b: USB Resume 10b: USB Operational 11b: USB Suspend A transition to UsbOperational from another state causes SOF generation to begin 1 ms later. The HCD may determine whether the HC has begun sending SOFs by reading the Start of Frame field of HC Interrupt Status. This field may be changed by the HC only in the UsbSuspend state. The HC may move from the USB Suspend state to the USB Resume state after the resume signal from a downstream port is detected. The HC enters USB Suspend after a software reset, whereas it enters USB Reset after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signal to downstream ports.
5	BLEn	R/W	Bulk List Enable. This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by the HCD, processing of the Bulk list does not occur after the next SOF. The HC checks this bit whenever it determines to process the list. When disabled, the HCD may modify the list. If HC Bulk Current ED is pointing to an ED to be removed, the HCD must advance the pointer by updating HC Bulk Current ED before the processing of the list is re-enabled.
4	CTLEn	R/W	Control List Enable. This bit is set to enable the processing of the Control list in the next Frame. If cleared by the HCD, the processing of the Control list does not occur after the next SOF. The HC must check this bit whenever it determines to process the list. When disabled, the HCD may modify the list. If HC Control Current ED is pointing to an ED to be removed, the HCD must advance the pointer by updating HC Control Current ED before re-enabling the processing of the list.
3	IEn	R/W	Isochronous Enable. This bit is used by the HCD to enable/disable the processing of isochronous EDs. While processing the periodic list in a Frame, the HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), the HC continues processing the EDs. If cleared (disabled), the HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	PLEn	R/W	Periodic List Enable. This bit is set to enable the processing of the periodic list in the next Frame. If cleared by the HCD, the processing of the periodic list does not occur after the next SOF. The HC must check this bit before it starts processing the list.
1-0	CTBSRT	R/W	Control Bulk Service Ratio. This specifies the service ratio between Control and Bulk EDs. Before processing any of the non-periodic lists, the HC must compare the ratio specified with its internal count on how many non-empty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, the HCD is responsible for restoring this value. CBSR No. of Control EDs Over Bulk EDs Served 0 1:1 1 2:1 2 3:1 3 4:1

Register Offset: 08h
Register Name: HC Command Status Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														SDORC		Reserved												ONCR	BLF	CTLF	HCTRS

The HC Command Status Register is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the Host Controller. To the Host Controller Driver, it appears to be a "write to set" register. The Host Controller must ensure those “written as '1'” bits become set in the register while those “written as ‘0’” bits remain unchanged in the register. The Host Controller Driver may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The Host Controller Driver has normal read access to all bits.

The Scheduling Overrun Count field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host Controller increments the counter and sets the Scheduling Overrun field in the HC Interrupt Status Register.

Bit	Name	Attribute	Description
31-18	Rsvd	RO	Reserved.
17-16	SDORC	RO	Scheduling Overrun Count. These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if Scheduling Overrun in HC Interrupt Status has already been set. This is used by the HCD to monitor any persistent scheduling problems.
15-4	Rsvd	RO	Reserved.
3	ONCR	R/W	Ownership Change Request. This bit is set by an OS HCD to request a change of control of the HC. When set, the HC will set the Ownership Change field in HC Interrupt Status. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	BLF	R/W	Bulk List Filled. This bit is used to indicate whether there are any TDs on the Bulk list. It is set by the HCD whenever it adds a TD to an ED in the Bulk list. When the HC begins to process the head of the Bulk list, it checks BF. As long as BLF is 0, the HC will not start processing the Bulk list. If BLF is 1, the HC will start processing the Bulk list and will set BF to 0. If the HC finds a TD on the list, then the HC will set BLF to 1, causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if the HCD does not set BLF, then BLF will still be 0 when the HC completes processing the Bulk list and Bulk list processing will stop.
1	CTLF	R/W	Control List Filled. This bit is used to indicate whether there are any TDs on the Control list. It is set by the HCD whenever it adds a TD to an ED in the Control list. When the HC begins to process the head of the Control list, it checks CTLF. As long as CTLF is 0, the HC will not start processing the Control list. If CF is 1, the HC will start processing the Control list and will set CLF to 0. If the HC finds a TD on the list, then the HC will set CTLF to 1, causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set CTLF, then CTLF will still be 0 when the HC completes processing the Control list and Control list processing will stop
0	HCTRS	R/W	Host Controller Reset. This bit is set by the HCD to initiate a software reset of the HC. Regardless of the functional state of the HC, it moves to the USB Suspend state in which most of the operational registers are reset except those stated otherwise; e.g., the Interrupt Routing field of HC Control, and no Host bus accesses are allowed. This bit is cleared by the HC upon the completion of the reset operation. The reset operation must be completed within 10 μs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signal should be asserted to its downstream ports.

Register Offset: 0Ch
Register Name: HC Interrupt Status Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	ONCS	Reserved																							RHSCS	FNOFS	Rsvd		RSDS	SFS	WBDHS	SDORS

This register provides status on various events that cause hardware interrupts. When an event occurs, the Host Controller sets the corresponding bit in this register. When a bit is set, a hardware interrupt is generated if the interrupt is enabled in the HC Interrupt Enable Register and the Master Interrupt Enable bit is set. The Host Controller Driver may clear specific bits in this register by writing '1' to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The Host Controller will never clear the bit.

Bit	Name	Attribute	Description
31	Rsvd	RO	Reserved.
30	ONCS	R/W	Ownership Change Status. This bit is set by the HC when the HCD sets the Ownership Change Request field in HC Command Status. This event, when unmasked, will always generate a System Management Interrupt (SMI_n) immediately.
29-7	Rsvd	RO	Reserved.
6	RHSCS	R/W	Root Hub Status Change Status. This bit is set when the contents of HC Rh Status or the contents of any of HC Rh Port Status [Number of Downstream Port] have changed.
5	FNOFS	R/W	Frame Number Overflow Status. This bit is set when the MSb of HC Fm Number (bit 15) changes values, from 0 to 1 or from 1 to 0, and after HCCA Frame Number has been updated.
4	Rsvd	RO	Reserved.
3	RSDS	R/W	Resume Detected Status. This bit is set when the HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when the HCD sets the USB Resume state.
2	SFS	R/W	Start of Frame Status. This bit is set by the HC at each start of a frame and after the update of HCCA Frame Number. The HC also generates an SOF token at the same time.
1	WBDHS	R/W	Write Back Done Head Status. This bit is set immediately after the HC has written HC Done Head to HCCA Done Head. Further updates of the HCCA Done Head will not occur until this bit has been cleared. The HCD should only clear this bit after it has saved the contents of HCCA Done Head.
0	SDORS	R/W	Scheduling Overrun Status. This bit is set when the USB schedule for the current Frame overruns and after the update of HCCA Frame Number. A scheduling overrun will also cause the Scheduling Overrun Count of HC Command Status to be incremented.

Register Offset: 10h
Register Name: HC Interrupt Enable Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MINTEn	ONCEn	Reserved																							RHSCEn	FNOFEn	Rsvd	RSDEn	SFEn	WBDHEn	SDOREn

Each enabled bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HC Interrupt Status Register. The HC Interrupt Enable Register is used to control those events to generate a hardware interrupt. When a bit is set in the HC Interrupt Status Register and the corresponding bit in the HC Interrupt Enable Register is set and the Master Interrupt Enable bit is set, a hardware interrupt is requested on the host bus.

Writing a '1' to a bit in this register sets the corresponding bit, whereas writing a '0' to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

Bit	Name	Attribute	Description
31	MINTEn	R/W	Master Interrupt Enable. A '0' written to this field is ignored by the HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by the HCD as a Master Interrupt Enable.
30	ONCEn	R/W	Ownership Change Enable. 0: Ignore. 1: Enable interrupt generation due to Ownership Change.
29-7	Rsvd	RO	Reserved.
6	RHSCEn	R/W	Root Hub Status Change Enable. 0: Ignore. 1: Enable interrupt generation due to Root Hub Status Change.
5	FNOFEn	R/W	Frame Number Overflow Enable. 0: Ignore. 1: Enable interrupt generation due to Frame Number Overflow.
4	Rsvd	RO	Reserved.
3	RSDEn	R/W	Resume Detected Enable. 0: Ignore. 1: Enable interrupt generation due to Resume Detect.
2	SFEn	R/W	Start of Frame Enable. 0: Ignore. 1: Enable interrupt generation due to Start of Frame.
1	WBDHEn	R/W	Write Back Done Head Enable. 0: Ignore. 1: Enable interrupt generation due to HC Done Head Writeback,
0	SDOREn	R/W	Scheduling Overrun Enable. 0: Ignore. 1: Enable interrupt generation due to Scheduling Overrun.

Register Offset: 14h
Register Name: HC Interrupt Disable Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MINTDis	ONCDis	Reserved																							RHSCDis	FNOFDis	UNRCEDis	RSDDis	SFDis	WBDHDis	SDORDis

Each disabled bit in the HC Interrupt Disable Register corresponds to an associated interrupt bit in the HC Interrupt Status Register. The HC Interrupt Disable Register is coupled with the HC Interrupt Enable Register. Thus, writing a '1' to a bit in this register clears the corresponding bit in the HC Interrupt Enable Register, whereas writing a '0' to a bit in this register leaves the corresponding bit in the HC Interrupt Enable Register unchanged. On read, the current value of the HcInterruptEnable register is returned.

Bit	Name	Attribute	Description
31	MINTDis	R/W	Master Interrupt Disable. A '0' written to this field is ignored by the HC. A '1' written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.
30	ONCDis	R/W	Ownership Change Disable. 0: Ignore. 1: Disable interrupt generation due to Ownership Change.
29-7	Rsvd	RO	Reserved.
6	RHSCDis	R/W	Root Hub Status Change Disable. 0: Ignore. 1: Disable interrupt generation due to Root Hub Status Change.
5	FNOFDis	R/W	Frame Number Overflow Disable. 0: Ignore. 1: Disable interrupt generation due to Frame Number Overflow.
4	UNRCEDis	R/W	Unrecoverable Error Disable. This event is not implemented. All writes to this bit will be ignored.
3	RSDDis	R/W	Resume Detected Disable. 0: Ignore. 1: Disable interrupt generation due to Resume Detect.
2	SFDis	R/W	Start of Frame Disable. 0: Ignore. 1: Disable interrupt generation due to Start of Frame.
1	WBDHDis	R/W	Write Back Done Head Disable. 0: Ignore. 1: Disable interrupt generation due to HcDoneHead Writeback.
0	SDORDis	R/W	Scheduling Overrun Disable. 0: Ignore. 1: Disable interrupt generation due to Scheduling Overrun.

12.5.2.3 Memory Pointer Partition

Register Offset: 18h

Register Name: HC HCCA Register

Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAHCTC																								Reserved							

The HC HCCA register contains the physical address of the Host Controller Communication Area. The Host Controller Driver determines the alignment restrictions by writing all 1s to HC HCCA and reading the contents of HC HCCA. The alignment is evaluated by examining the number of zeroes in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 must always return '0' when read. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.

Bit	Name	Attribute	Description
31-8	BAHCTC	R/W	This is the base address of the Host Controller Communication Area.
7-0	Rsvd	RO	Reserved.

Register Offset: 1Ch

Register Name: HC Period Current ED Register

Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRCRED																												Reserved			

The HC Period Current ED Register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Bit	Name	Attribute	Description
31-4	PRCRED	R/W	Period Current ED. This is used by the HC to point to the head of one of the Periodic lists that will be processed in the current Frame. The contents of this register are updated by the HC after a periodic ED has been processed. The HCD may read the contents in determining which ED is currently being processed at the time of reading.
3-0	Rsvd	RO	Reserved.

Register Offset: 20h
Register Name: HC Control Head ED Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTHED																												Reserved			

The HC Control Head ED Register contains the physical address of the first Endpoint Descriptor of the Control list.

Bit	Name	Attribute	Description
31-4	CTHED	R/W	Control Head ED. The HC traverses the Control list starting with the HC Control Head ED pointer. The contents are loaded from HCCA during the initialization of the HC.
3-0	Rsvd	RO	Reserved.

Register Offset: 24h
Register Name: HC Control Current ED Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTCRED																												Reserved			

The HC Control Current ED Register contains the physical address of the current Endpoint Descriptor of the Control list.

Bit	Name	Attribute	Description
31-4	CTCRED	R/W	Control Current ED. This pointer is advanced to the next ED after the present one is served. The HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, the HC checks CTLF in the HC Command Status Regster. If set, it copies the contents of HC Control Head ED to HC Control Current ED and clears the bit. If not set, it does nothing. The HCD is allowed to modify this register only when CTLEn in the HC Control Register is cleared. When set, the HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3-0	Rsvd	RO	Reserved.

Register Offset: 28h
Register Name: HC Bulk Head ED Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHED																												Reserved			

The HC Bulk Head ED Register contains the physical address of the first Endpoint Descriptor of the Bulk list.

Bit	Name	Attribute	Description
31-4	BHED	R/W	Bulk Head ED. The HC traverses the Bulk list starting with the HC Bulk Head ED pointer. The contents are loaded from HCCA during the initialization of the HC.
3-0	Rsvd	RO	Reserved.

Register Offset: 2Ch
Register Name: HC Bulk Current ED Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHCRD																												Reserved			

The HC Bulk Current ED Register contains the physical address of the current endpoint of the Bulk list. As the Bulk list will be served in a round-robin fashion, the endpoints will be ordered according to their insertion to the list.

Bit	Name	Attribute	Description
31-4	BCRED	R/W	Bulk Current ED. This is advanced to the next ED after the HC has served the present one. The HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, the HC checks the ControlListFilled of HcControl. If set, it copies the contents of HC Bulk Head ED to HC Bulk Current ED and clears the bit. If it is not set, it does nothing. The HCD is only allowed to modify this register when BLEn in the HC Control Register is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3-0	Rsvd	RO	Reserved.

Register Offset: 30h
Register Name: HC Done Head ED Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DH																												Reserved			

The HC Done Head Register contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, the Host Controller Driver should not need to read this register as its contents are periodically written to the HCCA.

Bit	Name	Attribute	Description
31-4	DH	R/W	Done Head. When a TD is completed, the HC writes the contents of HC Done Head to the Next TD field of the TD. The HC then overwrites the contents of HcDoneHead with the address of this TD. This is set to zero whenever the HC writes the contents of this register to HCCA. It also sets WBDHS in the HC Interrupt Status Register.
3-0	Rsvd	RO	Reserved.

12.5.2.4 Frame Counter Partition

Register Offset: 34h
Register Name: HC Fm Interval Register
Reset Value : 00002EDFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FINTVTG																Rsvd												FINTV			

The HC Fm Interval Register contains a 14-bit value which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the Host Controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustments on the FrameInterval by writing a new value over the present one at each SOF. This provides the programmability necessary for the Host Controller to synchronize with an external clocking resource and to adjust any unknown local clock offset.

Bit	Name	Attribute	Description
31	FINTVTG	R/W	Frame Interval Toggle. The HCD toggles this bit whenever it loads a new value to FrameInterval.
30-16	FSLDP	R/W	FS Largest Data Packet. This field specifies a value that is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15-14	Rsvd	RO	Reserved.
13-0	FINTV	R/W	Frame Interval. This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. The HCD should store the current value of this field before resetting the HC. By setting the HCTRS field in the HC Command Status Register as this will cause the HC to reset this field to its nominal value. The HCD may choose to restore the stored value upon the completion of the Reset sequence.

Register Offset: 38h
Register Name: HC Fm Remaining Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRMTG	Reserved																	FRM													

The HC Fm Remaining Register is a 14-bit down counter showing the bit time remaining in the current Frame.

Bit	Name	Attribute	Description
31	FRMTG	RO	Frame Remaining Toggle. This bit is loaded from the Frame Interval Toggle field in the HC Fm Interval Register whenever Frame Remaining reaches 0. This bit is used by the HCD for the synchronization between Frame Interval and Frame Remaining.
30-14	Rsvd	RO	Reserved.
13-0	FRM	RO	Frame Remaining. This counter is decremented at each bit time. When it reaches zero, it is reset by loading the Frame Interval value specified in the HC Fm Interval Register at the next bit time boundary. When entering the USB Operational state, the HC re-loads the content with the Frame Interval in the HC Fm Interval Register and uses the updated value from the next SOF.

Register Offset: 3Ch
Register Name: HC Fm Number Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FNB															

The HC Fm Number Register is a 16-bit counter. It provides a timing reference among events occurring in the Host Controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved.
15-0	FNB	RO	Frame Number. This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When the USB Operational state is entered, this will be incremented automatically. The contents will be written to HCCA after the HC has incremented the Frame Number at each frame boundary and sent a SOF but before the HC reads the first ED in that Frame. After writing to HCCA, the HC will set the Start of Frame in HC Interrupt Status.

Register Offset: 40h
Register Name: HC Periodic Start Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		PRS													

The Hc Periodic Start Register has a 14-bit programmable value that determines the earliest time the HC should start processing the periodic list.

Bit	Name	Attribute	Description
31-14	Rsvd	RO	Reserved.
13-0	PRS	R/W	Periodic Start After a hardware reset, this field is cleared. This is then set by the HCD during the HC initialization. The value is calculated roughly as 10% off from the HC Fm Interval Register. A typical value will be 3E67h. When HC Fm Remaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. The HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

Register Offset: 44h
Register Name: HC LS Threshold Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				LSTSH											

The HC LS Threshold register contains an 11-bit value used by the Host Controller to determine whether it is necessary to commit to the transfer of a maximum of 8-byte LS packets before EOF. Neither the Host Controller nor the Host Controller Driver is allowed to change this value.

Bit	Name	Attribute	Description
31-12	Rsvd	RO	Reserved.
11-0	LSTSH	R/W	LS Threshold. This field contains a value that is compared to the Frame Remaining field prior to initiating a Low Speed transaction. The transaction is started only if Frame Remaining ≥ this field. The value is calculated by the HCD with the consideration of transmission and set-up overhead.

12.5.2.5 Root Hub Partition

All registers included in this partition are dedicated to the USB Root Hub which is an integral part of the Host Controller though still a functionally separate entity. The HCD emulates USBD accesses to the Root Hub via a register interface. The HCD maintains many USB-defined hub features that are not required to be supported in hardware. For example, the Hub's Device, Configuration, Interface, and Endpoint Descriptors are maintained only in the HCD as well as some static fields of the Class Descriptor. The HCD also maintains and decodes the Root Hub's device address as well as other trivial operations that are better suited to software than hardware.

The Root Hub register interface is otherwise developed to maintain similarity of bit organization and operation to typical hubs that are found in the system. Below are four register definitions: HC Rh Descriptor A, HC Rh Descriptor B, HC Rh Status, and HC Rh Port Status [5:1]. Each register is read and written as a Dword. These registers are only written during initialization to correspond with the system implementation. The HC Rh Descriptor A and HC Rh Descriptor B registers should be implemented such that they are writable regardless of the HC USB state. HC Rh Status and HC Rh Port Status must be writable during the USB Operational state.

Register Offset: 48h
Register Name: HC Rh Discriptor A Register
Reset Value : 01001102h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POPGT								Reserved											NOCRPT	OCRPTM	DVT	NPSW	PSWM	NBDSTP								

The HC Rh Descriptor A Register is the first register of two describing characteristics of the Root Hub. Reset values are implementation-specific. All other fields are located in the HC Rh Descriptor A and HC Rh Descriptor B registers.

Bit	Name	Attribute	Description
31-24	POPGT	R/W	Power On to Power Good Time. This byte specifies the duration the HCD has to wait before a powered-on port of the Root Hub is accessed. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.
23-13	Rsvd	RO	Reserved.
12	NOCRPT	R/W	No Over Current Protection. This bit describes how the over-current status for the Root Hub ports is reported. When this bit is cleared, the Over Current Protection Mode field specifies global or per-port reporting. 0: Over-current status is reported collectively for all downstream ports. 1: No over-current protection supported.
11	OCRPTM	R/W	Over Current Protection Mode. This bit describes how the over-current status for the Root Hub ports is reported. At reset, this field should reflect the same mode as Power Switching Mode. This field is valid only if the No Over Current Protection field is cleared. 0: Over-current status is reported collectively for all downstream ports. 1: Over-current status is reported on a per-port basis.
10	DVT	RO	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	NPSW	R/W	No Power Switching. These bits are used to specify whether power switching is supported or ports are always powered. USB HC supports global power switching mode. When this bit is cleared, the Power Switching Mode specifies global or per-port switching. 0: Ports are power switched. 1: Ports are always powered on when the HC is powered on.

<table>
<tr><td>8</td><td>PSWM</td><td>R/W</td><td>Power Switching Mode.
This bit is used to specify how the power switching of the Root Hub ports is controlled. USB HC supports global power switching mode. This field is only valid if the No Power Switching field is cleared.
0: all ports are powered at the same time.
1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching.
If the Port Power Control Mask bit is set, the port responds only to port power commands (Set/Clear Port Power). If the port mask is cleared, the port is controlled only by the global power switch (Set/Clear Global Power).</td></tr>
<tr><td>7-0</td><td>NBDSTP</td><td>RO</td><td>Number Downstream Ports
These bits specify the number of downstream ports supported by the Root Hub.
Both of the HCs support three downstream ports.

In A version it can be programmed to 02h or 01h, HC0 is controlled by SB CFG 6C bit 0 and1, and HC1 is controlled by SB CFG 6C bit 2 and 3. The setting is tabulated below
<table>
<tr><th>NDP's value</th><th>SB CFG 6C bit0 or bit2</th><th>SB CFG 6C bit1 or bit3</th></tr>
<tr><td>01h</td><td>1</td><td>X</td></tr>
<tr><td>02h</td><td>0</td><td>1</td></tr>
<tr><td>03h</td><td>0</td><td>0</td></tr>
</table></td></tr>
</table>

Register Offset: 4Ch

Register Name: HC Rh Descriptor B Register

Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPWCTM																DVRM															

The HC Rh Descriptor B Register is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to configure the Root Hub.

Bit	Name	Attribute	Description
31-16	PPWCTM	R/W	Port Power Control Mask. Each bit indicates if a port is affected by a global power control command when Power Switching Mode is set. When set, the port's power state is only affected by per-port power control (Set/Clear Port Power). When cleared, the port is controlled by the global power switch (Set/Clear Global Power). If the device is configured to global switching mode (Power Switching Mode=0), this field is not valid. USB HC implements global power switching. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15
15-0	DVRM	R/W	Device Removable. Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15

Register Offset: 50h
Register Name: HC Rh Status Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRMWEn	Reserved													OCRIDC	LPSC	DRWE	Reserved													OCRID	LPS

The HC Rh Status Register is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written '0'.

Bit	Name	Attribute	Description
31	CRMWEn	WO	Clear Remote Wakeup Enable **(Write).** Writing a '1' clears Device Remove Wakeup Enable. Writing a '0' has no effect.
31-18	Rsvd	RO	Reserved.
17	OCRIDC	R/W	Over Current Indicator Change. This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
16	LPSC	R/W	Local Power Status Change (**Read**). The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. Set Global Power (**Write**). In global power mode (Power Switching Mode=0), this bit is written to '1' to turn on power to all ports (clear Port Power Status). In per-port power mode, it sets Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing a '0' has no effect.
15	DRWE	RO	Device Remote Wakeup Enable (**Read**). This bit enables a Connect Status Change bit as a resume event, causing an USB Suspend to USB Resume state transition and setting Resume Detected interrupt. 0: **Connect Status Change** is not a remote wakeup event. 1: **Connect Status Change** is a remote wakeup event. Set Remote Wakeup Enable (**Write**)**.** Writing a '1' sets Device Remove Wakeup Enable. Writing a '0' has no effect.
14-2	Rsvd	RO	Reserved.
1	OCRID	RO	Over Current Indicator. This bit reports over-current conditions when the global reporting is implemented. When set, an over-current condition exists. When cleared, all power operations are normal. If per-port over-current protection is implemented, this bit is always '0'
0	LPS	R/W	Local Power Status (**Read**). The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. Clear Global Power (**Write**). In global power mode (Power Switching Mode=0), This bit is written to '1' to turn off power to all ports (clear Port Power Status). In per-port power mode, it clears Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing a '0' has no effect.

Register Offset: 54h/58h
Register Name: HC Rh Port Status [2:1] Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											PRSC	POCRIDC	PSPSC	PEnSC	CNSC	Reserved						LSDVA	PPS	Reserved			PRS	POCI	PSS	PES	CCS

The HC Rh Port Status [2:1] registers are used to control and report port events on a per-port basis. Two HC Rh Port Status registers are implemented in this HC, respectively. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behaviour (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction is completed. Reserved bits should always be written as '0'. While the NDP of register 48h is 01h, the register 58 and register 5C will be read as 00000000h. While the NDP of register 48h is 02h, only register 5C is read as 00000000h.

Bit	Name	Attribute	Description
31-21	Rsvd	RO	Reserved.
20	PRSC	R/W	Port Reset Status Change. This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: port reset is not complete 1: port reset is complete
19	POCRIDC	R/W	Port Over Current Indicator Change. This bit is valid only if over-current conditions are reported on a per-port basis. This bit is set when Root Hub changes the Port Over Current Indicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: no change in Port Over Current Indicator 1: Port Over Current Indicator has changed
18	PSPSC	R/W	Port Suspend Status Change. This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resynchronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when Reset Status Change is set. 0: resume is not completed 1: resume completed
17	PEnSC	R/W	Port Enable Status Change. This bit is set when hardware events cause the Port Enable Status bit to be cleared. Changes from the HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: no change in Port Enable Status 1: change in Port Enable Status
16	CNSC	R/W	Connect Status Change. This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If Current Connect Status is cleared when a Set Port Reset, Set Port Enable, or Set Port Suspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0: no change in Current Connect Status. 1: change in Current Connect Status. ***Note:*** *If the Device Removable [NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.*
15-10	Rsvd	RO	Reserved.

9	LSDVA	R/W	Low Speed Device Attached (**Read**). This bit indicates the speed of the device attached to this port. When set, a Low-Speed device is attached to this port. When cleared, a Full Speed device is attached to this port. This field is valid only when the Current Connect Status is set. 0: full-speed device attached 1: low-speed device attached
8	PPS	R/W	Port Power Status (**Read**). This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an over-current condition is detected. The HCD sets this bit by writing Set Port Power or Set Global Power. The HCD clears this bit by writing Clear Port Power or Clear Global Power. Which power control switches will be enabled is determined by Power Switching Mode and Port Power Control Mask [NDP]. In global switching mode (Power Switching Mode=0), only Set/Clear Global Power controls this bit. In per-port power switching (Power Switching Mode=1), if the Port Power Control Mask [NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ Clear Global Power commands are enabled. When port power is disabled, Current Connect Status, Port Enable Status, Port Suspend Status, and Port Reset Status should be reset. 0: port power is off 1: port power is on Set Port Power (**Write**) The HCD writes a '1' to set the Port Power Status bit. Writing a '0' has no effect. ***Note:*** *This bit is always reads '1b' if power switching is not supported.*
7-5	Rsvd	RO	Reserved.
4	PRS	R/W	Port Reset Status (**Read**). When this bit is set by a write to Set Port Reset, port reset signaling is asserted. When reset is completed, this bit is cleared when Port Reset Status Change is set. This bit cannot be set if Current Connect Status is cleared. 0: port reset signal is not active 1: port reset signal is active Set Port Reset (**Write**). The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Reset Status, but instead sets Connect Status Change. This informs the driver that it attempted to reset a disconnected port.
3	POCI	R/W	Port Over Current Indicator (**Read**). This bit is only valid when the Root Hub is configured in such a way that over-current conditions are reported on a per-port basis. If per-port over-current reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an over-current condition exists on this port. This bit always reflects the over-current input signal 0: no over-current condition. 1: over-current condition detected. Clear Suspend Status (**Write**). The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if Port Suspend Status is set.
2	PSS	R/W	Port Suspend Status (**Read**). This bit indicates the port is suspended or in the resume sequence. It is set by a Set Suspend State write and cleared when Port Suspend Status Change is set at the end of the resume interval. This bit cannot be set if Current Connect Status is cleared. This bit is also cleared when Port Reset Status Change is set at the end of the port reset or when the HC is placed in the USB Resume state. If an upstream resume is in progress, it should propagate to the HC. 0: port is not suspended. 1: port is suspended. Set Port Suspend (**Write**). The HCD sets the Port Suspend Status bit by writing a '1' to this bit. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Suspend Status; instead it sets Connect Status Change. This informs the driver that it attempts to suspend a disconnected port.

1	PES	R/W	Port Enable Status (**Read**). This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an over-current condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes Port Enabled Status Change to be set. The HCD sets this bit by writing Set Port Enable and clears it by writing Clear Port Enable. This bit cannot be set when Current Connect Status is cleared. This bit is also set, if not already, at the completion of a port reset when Reset Status Change is set or a port suspend when Suspend Status Change is set. 0: port is disabled. 1: port is enabled. Set Port Enable (**Write**). The HCD sets Port Enable Status by writing a '1'. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Enable Status, but instead sets Connect Status Change. This informs the driver that it attempts to enable a disconnected port.
0	CCS	R/W	Current Connect Status (**Read**). This bit reflects the current state of the downstream port. 0: no device connected. 1: device connected. Clear Port Enable (**Write**). The HCD writes a '1' to this bit to clear the Port Enable Status bit. Writing a '0' has no effect. Current Connect Status is not affected by any write. ***Note:*** *This bit is always read as '1b' when the attached device is non-removable (Device Removeable [NDP]).*

12.5.2.6 Legacy Support Registers

Four operational registers are used to provide the legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100h.

Table 12.1: Legacy Support Registers

Offset	Register	Description
100h	HC eControl	Used to enable and control the emulation hardware and report various status informations.
104h	HC eInput	Emulation side of the legacy Input Buffer register.
108h	HC eOutput	Emulation side of the legacy Output Buffer register where keyboard and mouse data are written by software.
10Ch	HC eStatus	Emulation side of the legacy Status register.

Three of the operational registers (HC eStatus, HC eInput and HC eOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table 12.1.

Table 12.2: Emulated Registers

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60h	IN	HC eOutput	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	HC eInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HC eStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HC eInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

Register Offset: 100h
Register Name: HC eControl Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																							A20S	IRQ12A	IRQ1A	GA20S	ETIRQEn	IRQEn	CTPD	EMLINT	EMLEn

Bit	Name	Attribute	Description
31-9	Rsvd	RO	Reserved.
8	A20S	R/W	A20 State. Indicates current state of Gate A20 on keyboard controller. Used to compare value to 60h when Gate A20 Sequence is active.
7	IRQ12A	R/W	IRQ12 Active Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
6	IRQ1A	R/W	IRQ1 Active. Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
5	GA20S	R/W	Gate A20 Sequence. Set by the HC when a data value of D1h is written to I/O port 64h; cleared by the HC on writes to I/O port 64h of any value other than D1h.
4	ETIRQEn	R/W	External IRQ Enable. When set to 1, IRQ1 and IRQ12 from the keyboard controller cause an emulation interrupt. The function controlled by this bit is independent of the setting of the Emulation Enable bit in this register.
3	IRQEn	R/W	IRQ Enable. When set, the HC generates IRQ1 or IRQ12 as long as the Output Full bit in HC eStatus is set to 1. If the Aux Output Full bit of HC eStatus is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
2	CTPD	R/W	Character Pending. When set, an emulation interrupt is generated when the Output Full bit in the HC eStatus Register is set to 0.
1	EMLINT	RO	Emulation Interrupt. This bit is a static decode of the emulation interrupt condition
0	EMLEn	R/W	Emulation Enable. When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.

Register Offset: 104h
Register Name: HC eInput Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								IPD							

Bit	Name	Attribute	Description
31-8	Rsvd	RO	Reserved.
7-0	IPD	R/W	Input Data This register holds data that is written to I/O ports 60h and 64h. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

Register Offset: 108h
Register Name: HC eOutnput Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								OPD							

Bit	Name	Attribute	Description
31-8	Rsvd	RO	Reserved.
7-0	OPD	R/W	Output Data This register hosts data that is returned when an I/O read of port 60h is performed by application software. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the Output Full bit in the HC eStatus Register is set to 0.

Register Offset: 10Ch
Register Name: HC eStatus Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PRT	TOUT	AOF	IHBSW	CD	F	IPF	OPF

Bit	Name	Attribute	Description
31-8	Rsvd	RO	Reserved.
7	PRT	R/W	Parity. Indicates parity error on keyboard/mouse data.
6	TOUT	R/W	Time-out. Used to indicate a time-out
5	AOF	R/W	Aux Output Full. IRQ12 is asserted whenever this bit is set to 1 and Output Full is set to 1 and the IRQEn bit is set.
4	IHBSW	R/W	Inhibit Switch. This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3	CD	R/W	Cmd Data. The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h
2	F	R/W	Flag. Nominally used as a system flag by software to indicate a warm or cold boot.
1	IPF	R/W	Input Full. Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0	OPF	R/W	Output Full. The HC sets this bit to 0 on a read of I/O port 60h. If IRQEn is set and Aux Output Full is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and Aux Output Full is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and Character Pending in the HC eControl Register is set to 1, an emulation interrupt condition exists. The contents of the HC eStatus Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects.

12.5.3 EHCI Configuration Space

12.5.3.1 USB2.0 Configuration Space

Register Offset: 01h – 00h
Register Name: Vendor ID Register
Reset Value : 17F3h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VID															

Bit	Name	Attribute	Description
15-0	VID	RO	Vendor ID.

Register Offset: 03h – 02h
Register Name: Device ID Register
Reset Value : 6061h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID															

Bit	Name	Attribute	Description
15-0	DID	RO	Device ID.

Register Offset: 05h – 04h
Register Name: Command Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SDTEn	Reserved					PCIMEn	MEn	IOEn

Bit	Name	Attribute	Description
15-9	Rsvd	RO	Reserved bits. These bits are always 0.
8	SDTEn	R/W	SERR_n (Response) Detection Enable bit If set to 1, the EHC asserts SERR_n when it detects an address parity error. SERR_n is not asserted if this bit is 0.
7-3	Rsvd	RO	Reserved bits These bits are always 0.
2	PCIMEn	R/W	PCI Master Enable If set to 1, the EHC is enabled to run PCI master cycles.
1	MEn	R/W	Memory Enable. If set to 1, the EHC is enabled to respond as a target to memory cycles.

0	IOEn	RO	I/O Enable. This bit is always 0.

Register Offset: 07h – 06h
Register Name: Status Register
Reset Value : 0280h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTPRE	SERRS	RMAS	RTAS	SNTAS	DVST		DPRP	Reserved				INTS	Reserved		

Bit	Name	Attribute	Description
15	DTPRE	RO	Detected Parity Error. This bit is always 0.
14	SERRS	R/W	SERR_n Status. This bit is set to 1 whenever the EHC detects a PCI address parity error. Cleared by writing a 1 to it.
13	RMAS	R/W	Received Master Abort Status. This bit is set to 1 when the EHC receives a master-abort status on a PCI bus memory cycle. Cleared by writing a 1 to it.
12	RTAS	R/W	Received Target Abort Status. This bit is set to 1 when the EHC receives a target-abort status on a PCI bus memory cycle. Cleared by writing a 1 to it.
11	SNTAS	R/W	Signaled Target Abort Status. This bit is set to 1 when the EHC responds to a memory cycle with a target abort. Cleared by writing a 1 to it.
10-9	DVST	RO	DEVSEL_n timing. Read-only bits indicating DEVSEL_n timing when performing a positive decode. Since DEVSEL_n is asserted to meet the medium timing, these bits are encoded as 01b.
8	DPRP	R/W	Data Parity Reported. Set to 1 if the Parity Error Response bit is set, and the EHC detects PERR_n asserted while acting as PCI master (whether PERR_n was driven by the EHC or not).
7-4	Rsvd	RO	Reserved bits These bits are always 0.
3	INTS	R/O	Interrupt Status. This bit reflects the state of the interrupt in the device.
2-0	Rsvd	RO	Reserved bits. These bits are always 0

Register Offset: 08h
Register Name: Revision ID Register
Reset Value : 00h

7	6	5	4	3	2	1	0
FTRVL							

Bit	Name	Attribute	Description
7-0	FTRVL	RO	Functional Revision Level.

Register Offset: 0Bh – 09h
Register Name: Class Code Register
Reset Value : 0C0320h

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCLS								SUBCLS								PRGINTF							

Bit	Name	Attribute	Description
23-16	BCLS	RO	Base Class. The Base Class is 0Ch (Serial Bus Controller).
15-8	SUBCLS	RO	Sub Class. The Sub Class is 03h (Universal Serial Bus).
7-0	PRGINTF	RO	Programming Interface. The Programming Interface is 20h (USB2.0).

Register Offset: 0Ch
Register Name: Cache Line Size Register
Reset Value : 00h

7	6	5	4	3	2	1	0
CCHLSZ							

Bit	Name	Attribute	Description
7-0	CCHLSZ	R/W	Cache Line Size. This register identifies the system cache line size in units of 32-bit words. The ECH will only store the value of bit 3 in this register since the cache line size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

Register Offset: 0Dh
Register Name: Latency Timer Register
Reset Value : 00h

7	6	5	4	3	2	1	0
LTCTimer							

Bit	Name	Attribute	Description
7-0	LTCTimer	R/W	Latency Timer. This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles.

Register Offset: 0Eh
Register Name: Header Type Register
Reset Value : 00h

7	6	5	4	3	2	1	0
HT							

Bit	Name	Attribute	Description
7-0	HT	RO	Header Type Register. This register identifies the type of the predefined header in the configuration space. Since the EHC is a single function device and not a PCI-to-PCI bridge, the byte should be read as 00h.

Register Offset: 13h – 10h
Register Name: Base Address Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAD																				Reserved											

Bit	Name	Attribute	Description
31-12	BAD	R/W	Base Address. POST writes the value of the memory base address to this register.
11-0	Rsvd	RO	Always 0.

Register Offset: 2Dh – 2Ch
Register Name: Subsystem Vendor ID Register
Reset Value : 17F3h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSVDID															

Bit	Name	Attribute	Description
15	SSVDID	R/WS	Subsystem Vendor ID. Set the value in this field to identify the subsystem vendor ID. Before writing to this field, write-protect bits in register 40h bit 1:0 must be disabled.

Register Offset: 2Fh – 2Eh
Register Name: Subsystem ID Register
Reset Value : 6061h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSID															

Bit	Name	Attribute	Description
15	SSID	R/WS	Subsystem ID. Set the value in this field to identify the subsystem ID. Before writing to this field, write-protect bits in register 40h bit[1:0] must be disabled.

Register Offset: 3Dh – 3Ch
Register Name: Interrupt Control Register
Reset Value: 01XXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTP								INTL							

Bit	Name	Attribute	Description
15-8	INTP	R	Interrupt Pin. Use INT_A.
7-0	INTL	R/W	Interrupt Line. Index Interrupt Vector.

Register Offset: 3Eh
Register Name: Minimun Grant Register
Reset Value : 00h

7	6	5	4	3	2	1	0
MINGNT							

Bit	Name	Attribute	Description
7-0	MINGNT	RO	Minimum Grant. This register specifies the desired settings for how long of a burst EHC needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Offset: 3Fh
Register Name: Max Latency Register
Reset Value : 00h

7	6	5	4	3	2	1	0
MAXLAT							

Bit	Name	Attribute	Description
7-0	MAXLAT	RO	Maximum Latency. This register specifies the desired setting for how often the EHC needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Offset: 43h – 40h
Register Name: Operational Mode Enable Register
Reset Value : 00000080h
Recommend Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PTC			Rsvd			WSRP	

Bit	Name	Attribute	Description
31-8	Rsvd	R/W	Reserved. These bits are only used for test-mode. Changes to these bits will cause undefined behavior.
7-5	PTC	R/W	PCIFIFO Threshold Control. These bits are used to control the PCIFIFO threshold level. When PCIFIFO threshold is reached, OUT cycle will be driven by the EHC. 000 : PCIFIFO threshold is set to 128 bytes 001 : PCIFIFO threshold is set to 256 bytes 010 : PCIFIFO threshold is set to 384 bytes 011 : PCIFIFO threshold is set to 512 bytes 100 : PCIFIFO threshold is set to 640 bytes 101 : PCIFIFO threshold is set to 768 bytes 110 : PCIFIFO threshold is set to 896 bytes 111 : PCIFIFO threshold is set to 1024 bytes
4-2	Rsvd	R/W	Reserved. These bits are only used for test-mode. Changes to these bits will cause undefined behavior.
1-0	WSRP	R/W	Write Special Registers Protect. These registers protect write-special registers. 10: Registers can be written Others: Register cannot be written

Register Offset: 60h
Register Name: USB Release Number Register
Reset Value : 20h

7	6	5	4	3	2	1	0
USBRN							

Bit	Name	Attribute	Description
7-0	USBRN	RO	USB Release Number. This register is hardwired to 20h to indicate the EHC follows USB 2.0 Spec.

Register Offset: 61h
Register Name: Frame Length Adjustment Register
Reset Value : 20h

7	6	5	4	3	2	1	0
Reserved				FLTV			

Bit	Name	Attribute	Description
7-6	Rsvd	RO	Reserved. These registers are always 0.
5-0	FLTV	R/W	Frame Length Timing Value. Each decimal value change to this register corresponds to 16-bit times for high-speed bus.

Register Offset: 63h – 62h
Register Name: Port Wake Capability Register
Reset Value : 007Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PWCM							PWI

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved. These registers are always 0.
7-1	PWCM	R/W	Port Wake Up Capability Mask. Bit positions 1 through 6 correspond to a physical port implemented on this host controller. A one in a bit position indicates that a device connected below the port can be enabled as a wake-up device.
0	PWI	R/W	Port Wake Implemented. A one in this bit indicates whether the register is implemented.

Register Offset: 65h – 64h
Register Name: USB1.1 Port Override Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PWCM							PWI

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved. These registers are always 0.
7-1	PWCM	R/W	USB1.1 Port7-1 Owner. Bit positions 1 through 5 correspond to a physical port implemented on this host controller. A one in a bit position indicates that a device connected below the port will always be routed to USB1.1 host controller.
0	PWI	RO	USB1.1 Port 0 Owner. Port 0 for the EHC must never be programmed to the USB1.1 because this port is used as debug port.

Register Offset: 73h – 70h
Register Name: USB Legacy Support Extended Capability Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							HC OS	Reserved							HC OS	NEHCIECP								CID							

Bit	Name	Attribute	Description
31-25	Rsvd	RO	Reserved. These registers are always 0.
24	HCOS	R/W	HC Owned Semaphore. System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit is read as one and the HC Owned Semaphore bit read as zero.
23-17	Rsvd	RO	Reserved. These registers are always 0.
16	HCOS	R/W	HC Owned Semaphore. Set this bit to establish ownership of the EHCI controller. System will set this bit to a zero in response to a request for ownership of the EHCI controller by system software.
15-8	NEHCIECP	RO	Next EHCI Extended Capability Pointer. A value of 00h indicates the end of the extended capability list.
7-0	CID	RO	Capability ID. A value of 01h identifies the capability as Legacy Support.

Register Offset: 77h – 74h
Register Name: USB Legacy Support Control/Status Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMIBAR	SMIPCIC	SMIOSOC	Reserved							SMIAA	SMIHSE	SMIFLR	SMIPCD	SMIUSBE	SMIUSBC	SMIBAREn	SMIPCICEn	SMIOSOCEn	Reserved							SMIAAEn	SMIHSEEn	SMIFLREn	SMIPCDEn	SMIUSBEEn	SMIUSBCEn

Bit	Name	Attribute	Description
31	SMIBAR	R/WC	SMI on BAR. This bit is set to one whenever the Base Address Register (BAR) is written.
30	SMIPCIC	R/WC	SMI on PCI Command. This bit is set to one whenever the PCI Command Register is written.
29	SMIOSOC	R/WC	SMI on OS Ownership Change. This bit is set to one whenever the HC OS Owned Semaphore bit in the USBLEGSUP register is changed.
28-22	Rsvd	RO	Reserved. These registers are always 0.
21	SMIAA	RO	SMI on Async Advance. Shadow bit of the Interrupt on the Async Advance bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
20	SMIHSE	RO	SMI on Host System Error. Shadow bit of Host System Error bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
19	SMIFLR	RO	SMI on Frame List Rollover. Shadow bit of Frame List Rollover bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
18	SMIPCD	RO	SMI on Port Change Detect. Shadow bit of Port Chance Detect bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
17	SMIUSBE	RO	SMI on USB Error. Shadow bit of USB Error Interrupt (USBERRINT) bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
16	SMIUSBC	RO	SMI on USB Complete. Shadow bit of USB Interrupt (USBINT) bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
15	SMIBAREn	R/W	SMI on BAR Enable.
14	SMIPCICEn	R/W	SMI on PCI Command Enable.
13	SMIOSOCEn	R/W	SMI on OS Ownership Change Enable.
12-6	Rsvd	RO	Reserved. These registers are always 0.
5	SMIAAEn	R/W	SMI on Async Advance Enable.
4	SMIHSEEn	R/W	SMI on Host System Error Enable.
3	SMIFLREn	R/W	SMI on Frame List Rollover Enable.
2	SMIPCDEn	R/W	SMI on Port Change Detect Enable.
1	SMIUSBEEn	R/W	SMI on USB Error Enable.
0	SMIUSBCEn	R/W	SMI on USB Complete Enable.

Register Offset: 7Bh – 78h
Register Name: USB Legacy Support Enable/Status Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd										LP8-1OC																PMCSCEn	ASEnCEn	PSEnCEn	CFCEn	HCHCEn	HCSCEn

Bit	Name	Attribute	Description
31-30	Rsvd	RO	Reserved. These registers are always 0.
29-22	LP8-1OC	R/WC	Legacy port 8-1 owner Change. Bit positions 22 through 29 correspond to a physical port on this host controller. A one in a bit position indicates that a device owner is changed
21	PMCSC	R/WC	PMCS Change. This bit is set to one whenever the PMCS is changed.
20	ASEnC	R/WC	Asynchronous Schedule Enable Change. This bit is set to one whenever the Asynchronous Schedule Enable bit is changed.
19	PSEnC	R/WC	Periodic Schedule Enable Change. This bit is set to one whenever the Peridic Schedule Enable bit is changed.
18	CFC	R/WC	Configure Flag Change. This bit is set to one whenever the Configure Flag bit is changed.
17	HCHC	R/WC	HCHalted Change. This bit goes to one whenever the HCHalted register makes a 0b to 1b transition.
16	HCRC	R/WC	HCRESET Change. This bit goes to one whenever the HCRESET register makes a 0b to 1b transition.
15-14	Rsvd	RO	Reserved. These registers are always 0.
13-6	LP7-0OCEn	R/W	Legacy Port 7-0 Owner Change Enable.
5	PMCSCEn	R/W	PMCS Change Enable.
4	ASEnCEn	R/W	Asynchronous Schedule Enable Change Enable.
3	PSEnCEn	R/W	Periodic Schedule Enable Change Enable.
2	CFCEn	R/W	Configure Flag Change Enable.
1	HCHCEn	R/W	HCHalted Change Enable.
0	HCSCEn	R/W	HCRESET Change Enable.

12.5.4 EHCI Operational Registers

The base address of these registers is programmable by the memory base address register (EHC PCI configuration register offset 10h – 13h). These registers should be written as DWORD. Bytes access to these registers may have unpredictable effects.

12.5.4.1 Host Controller Capability Register

Register Offset: 00h
Register Name: Capability Register Length Register
Reset Value : 20h

7	6	5	4	3	2	1	0
CRL							

Bit	Name	Attribute	Description
7-0	CRL	RO	Capability Register Length. This register indicates to the length of the host controller capability register.

Register Offset: 03h – 02h
Register Name: USB1.1 Port Override Register
Reset Value : 0100h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCIVN															

Bit	Name	Attribute	Description
15-0	HCIVN	RO	Host Controller Interface Version Number. This register indicates the EHC supports the EHCI Spec Revision 1.0.

Register Offset: 07h – 04h
Register Name: Structure Parameters Register
Reset Value : 00103308h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DPN				Reserved				N_CC				N_PCC				Reserved				N_PORTS			

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. These registers are always 0.
23-20	DPN	RO	Debug Port Number. This register identifies the first port as the debug port.
19-16	Rsvd	RO	Reserved. These registers are always 0.
15-12	N_CC	RO	Number of Companion Controller (N_CC). This field indicates the number of companion controllers associated with this USB2.0 host controller.
11-8	N_PCC	RO	Number of Ports per Companion Controller (N_PCC). This field indicates the number of ports supported per companion host controller.
7-4	Rsvd	RO	Reserved. These registers are always 0.
3-0	N_PORTS	RO	Number of Ports (N_PORTS). This field indicates the number of ports supported on this host controller.

Register Offset: 0Bh – 08h
Register Name: Capability Parameters Register
Reset Value : 00800070h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																EECP								IST				Rsvd	ASOC	Rsvd	

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. These registers are always 0.
15-8	EECP	RO	EHCI Extend Capabilities Pointer (EECP). This field indicates the existence of a capability list.
7-4	IST	R/WS	Isochronous Scheduling Threshold. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule.
3	Rsvd	RO	Reserved. This register is always 0.
2	ASOC	R/WS	Asynchronous Schedule Park Capability. If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule.
1-0	Rsvd	RO	Reserved. These registers are always 0.

12.5.4.2 Host Controller Operational Register

Register Offset: 23h – 20h
Register Name: USB2.0 Command Register
Reset Value : 00080000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ITC								Rsvd				ASPMC	Rsvd	ASPMEn		LHCR	INT_AAD	ASEn	PSEn	Rsvd		HCRESET	RS

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. These registers are always 0.
23-16	ITC	R/W	Interrupt Threshold Control. This field is used by system software to select the maximum rate at which the host controller will issue interrupts.
15-12	Rsvd	RO	Reserved. These registers are always 0.
11	ASPMEn	R/W	Asynchronous Schedule Park Mode Enable. If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1h and is R/W. Software uses this bit to enable or disable Park mode.
10	Rsvd	RO	Reserved. This register is always 0.
9-8	ASPMC	R/W	Asynchronous Schedule Park Mode Count. If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 3h and is R/W. This field contains a count to the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the asynchronous schedule.
7	LHCR	R/W	Light Host Controller Reset. It allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers.
6	INT_AAD	R/W	Interrupt on Async Advance Doorbell. This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule.
5	ASEn	R/W	Asynchronous Schedule Enable. This bit controls whether the host controller skips processing the Asynchronous Schedule.
4	PSEn	R/W	Periodic Schedule Enable. This bit controls whether the host controller skips processing the Periodic Schedule.
3-2	Rsvd	RO	Reserved. These registers are always 0.
1	HCRESET	R/W	Host Controller Reset (HCRESET). This control bit is used by software to reset the host controller.
0	RS	R/W	Run/Stop (RS) When set to a 1, the host controller proceeds with execution of the schedule.

Register Offset: 27h – 24h
Register Name: USB2.0 Status Register
Reset Value : 00001000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																ASS	PSS	RCLM	HCHalted	Reserved						INT_AA	HSERR	FLRL	PCD	USBERRINT	USBINT

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. These registers are always 0.
15	ASS	RO	Asynchronous Schedule Status. This bit reports the current real status of the Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled.
14	PSS	RO	Periodic Schedule Status. This bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled.
13	RCLM	RO	Reclamation. This bit is used to detect an empty asynchronous schedule.
12	HCHalted	RO	Host Controller Halted (HCHalted). This bit is a zero whenever the Run/Stop bit is a one. The Host Controller sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware.
11-6	Rsvd	RO	Reserved. These registers are always 0.
5	INT_AA	R/WC	Interrupt on Async Advance. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USB2CMD register.
4	HSERR	R/WC	Host System Error. The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module.
3	FLRL	R/WC	Frame List Rollover. The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero.
2	PCD	R/WC	Port Change Detect. The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transaction detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	USBERRINT	R/WC	USB Error Interrupt (USBERRINT). The Host Controller sets this bit to 1 when completion of a USB transaction results in an error condition.
0	USBINT	R/WC	USB Interrupt (USBINT). The Host Controller sets this bit to 1 one the completion of a USB transaction, which result in the retirement of a Transfer Descriptor that had its IOC bit set.

Register Offset: 2Bh – 28h
Register Name: USB2.0 Interrupt Enable Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										INT_AAEn	HSERREn	FLRLEn	PCDEn	USBERRINTEn	USBINTEn

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. These registers are always 0.
5	INT_AAEn	R/W	Interrupt on Async Advance Enable. When this bit is a one and the Interrupt on the Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on the Async Advance bit.
4	HSERREn	R/W	Host System Error Enable. When this bit is a one and the Host System Error Status bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	FLRLEn	R/W	Frame List Rollover Enable. When the Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit
2	PCDEn	R/W	Port Change Detect Enable. When this bit is a one and the Port Chang Detect bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	USBERRINTEn	R/W	USB Error Interrupt Enable. When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	USBINTEn	R/W	USB Interrupt Enable. When this bit is a one and the USBINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

Register Offset: 2Fh – 2Ch
Register Name: USB2.0 Frame Index Register
Reset Value : 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		FI													

Bit	Name	Attribute	Description
31-14	Rsvd	RO	Reserved. These registers are always 0.
13-0	FI	R/W	Frame Index. The value in this register is incremented at the end of each time frame.

Register Offset: 37h – 34h
Register Name: Periodic Frame List Base Address Register
Reset Value : undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																				Reserved											

Bit	Name	Attribute	Description
31-12	BA	R/W	Base Address. These bits correspond to memory address [31:12].
11-0	Rsvd	RO	Reserved. These registers are always 0.

Register Offset: 3Bh – 38h
Register Name: Current Asynchronous List Address Register
Reset Value : undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LP																											Reserved			

Bit	Name	Attribute	Description
31-5	LP	R/W	Link Pointer. These bits correspond to memory address [31:5].
4-0	Rsvd	RO	Reserved. These registers are always 0.

Register Offset: 63h – 60h
Register Name: Configured Flag Register
Reset Value : undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															CF

Bit	Name	Attribute	Description
31-1	Rsvd	RO	Reserved. These registers are always 0.
0	CF	R/W	Configure Flag (CF). Host software sets this bit as the last action in its process of configuring the Host Controller. Writing a one to this register will route all ports to this host controller.

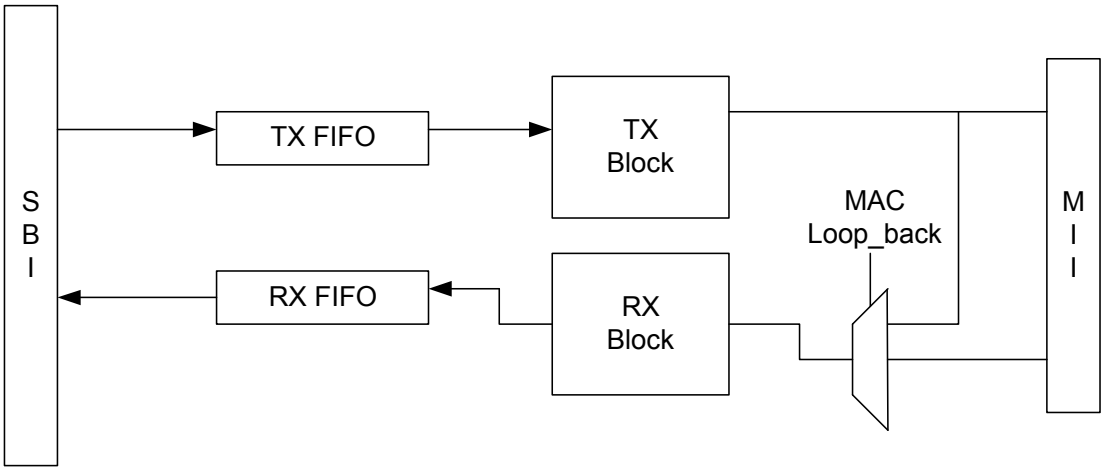
Register Offset: 67h – 64h
Register Name: Port 0 Status and Control Register
Register Offset: 68-6Bh
Register Name: Port 1 Status and Control Register
Reset Value : 00002000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									WKOC_E	WKDSCNNT_E	WKCCNT_N	PTC				Rsvd		PO	PP	LS		Rsvd	PRESET	SSPND	FPRS	OCRC	OCRA	P_EDC	P_ED	CNNTSC	CRCNNTS

Bit	Name	Attribute	Description
31-23	Rsvd	RO	Reserved. These registers are always 0.
22	WKOC_E	R/W	Wake on Over-current Enable (WKOC_E). Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events.
21	WKDSCNNT_E	R/W	Wake on Disconnect Enable (WKDSCNNT_E). Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
20	WKCNNT_E	R/W	Wake on Connect Enable (WKCNNT_E). Writing this bit to a one enables the port to be sensitive to device connects as wake-up events.
19-16	PTC	R/W	Port Test Control. When this field is zero, the port does NOT come into operation in test mode.
15-14	Rsvd	RO	Reserved. These registers are always 0.
13	PO	R/W	Port Owner. This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. Software writes a one to this bit when the attached device is not a high-speed device.
12	PP	RO	Port Power (PP). The Host Controller does not have port power control switches. Each port is hard-wired to power.

11-10	LS	RO	Line Status. These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines.
9	Rsvd	RO	Reserved. This bit is always 0.
8	PRESET	R/W	Port Reset. When software writes a one to this bit, the bus reset sequence as defined in the USB Spec Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence.
7	SSPND	R/W	Suspend. Software writes a one to this bit to suspend the downstream port. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when software sets the Force Port Resume from 1 to 0 or sets the Port Reset bit to 1.
6	FPRS	R/W	Force Port Resume. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. A write of zero to this bit will force the downstream port to follow the resume sequence defined in the sequence documented in the USB Spec Revision 2.0.
5	OCRC	R/WC	Over-current Change. This bit gets set to a one when there is a change to Over-current Active.
4	OCRA	RO	Over-current Active. 0: This port does not have an over-current condition. 1: This port has an over-current condition.
3	P_EDC	R/WC	Port Enable/Disable Change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 pointer.
2	P_ED	R/W	Port Enable/Disabled. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition or by host software.
1	CNNTSC	R/WC	Connect Status Change. 1: Change in Current Connect Status. 0: No change.
0	CRCNNTS	R/W	Current Connect Status. This value reflects the current connect status of the port.

13. Fast Ethernet Control Unit



SBI : System Bus Interface

MAC Block Diagram

13.1 RX Descriptor Format

15 ... 3	2	1	0
DRST			
DRLEN			
DRBP			0
DRBP[31:16]			
DRNX			0
DRNX[31:16]			
HIDX[5:0]			
Reserve2			
Reserve3			

1. DRST

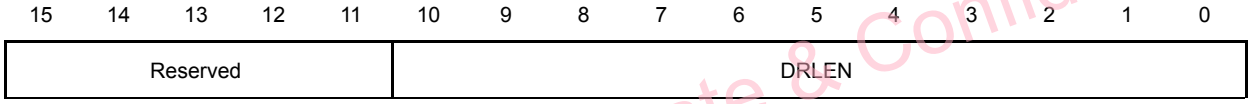
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	RXOK	Reserved		PHY ERR	DRI BBLE	OBL	LONG	RUNT	CRC ERR	BROAD CAST	MULTI CAST	MCH	MIDH	MID	

The RX circuit will stop receiving packets if the Owner bit=0.
DRST[14:0]: RX status. The MAC will update the RX status field after frame receiving is complete.

Bit	Name	Description
15	O	Owner bit. Set 1: the MAC. Set 0: the CPU.
14	RXOK	RX successful. This bit indicates that the packet was received successfully without errors. It includes: (1) RX_ER = 0 (MII interface). (2) Ignore DRIBBLE status. (3) No over buffer length. (4) Without CRC errors. (5) Not a LONG packet. (6) Not a RUNT packet. (7) No FIFO Full.

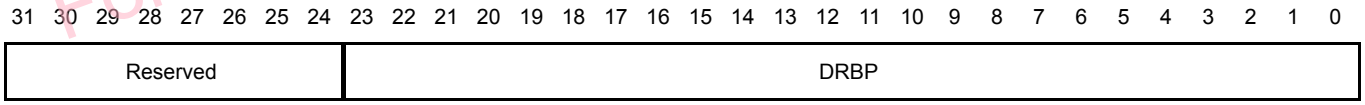
13-12	Rsvd	Reserved.
11	PHYERR	PHY RX Error packet. Reading “1” means that an error occurred in receiving packets on the MII interface.
10	DRIBBLE	Dribble packet. Reading “1” means the received packet is a dribble packet.
9	OBL	Over Buffer Length. Reading “1” means the received packet length > buffer maximum length.
8	LONG	Long packet. Reading “1” means the received packet length > maximum packet length.
7	RUNT	Runt packet. Reading “1” means the received packet length < 64 bytes.
6	CRCERR	CRC Error packet. Reading “1” means receiving a packet with CRC errors.
5	BROADCAST	It indicates that the received packet is a broadcast packet.
4	MULTICAST	It indicates that the received packet is a multicast packet.
3	MCH	Multicast Hit. It indicates that the received packet hits one of the hash-table bits.
2	MIDH	MID table is hit.
1-0	MID	Index of matched MIDx. These two bits indicate that the received packet hits one of the MID groups.

2. DRLEN



Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DRLEN	The size of the received frame.

3. DRBP



Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRBP	RX Data Buffer Pointer. This is a 32-bit address pointer and DRBP0 is always 0.

4. DRNX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DRNX																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRNX	RX Next Frame Descriptor Pointer. This is a 32-bit descriptor address pointer and DRNX0 is always 0. This field must be pointed to next descriptor start address or its start address.

5. HIDX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										HIDX					

Bit	Name	Description
15-6	Rsvd	Reserved.
5-0	HIDX	HIDX[5:0] is a hash index. If MCR1[14] is set to 1, the hash index number will be written into the RX description.

6. Reserve 2.
7. Reserve 3.

Notes:
1. The RX descriptor start address and data buffer start address must be double-word alignment.
2. The RX packet will be filtered out if its length is less than 6 (not complete DA information).

13.2 TX Descriptor Format

15	3	2	1	0
DTST				
DTLEN				
DTBP				
DTBP[31:16]				
DTNP				0
DTNP[31:16]				

1. DTST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	TXOK	DIS CRC	Reserved						TXFUR	LATEC	EXCEE DC	COLCNT			

The TX circuit will stop transmitting packets if the Owner bit=0
DTST[14:0]: TX status and packet control. The MAC will update the TX status field after frame transmission is complete. The control bit is for each packet usage.

Bit	Name	Description
15	O	Owner bit. Set 1: the MAC. Set 0: the CPU.
14	TXOK	TX packet successful. This bit indicates that the packet was transmitted successfully without errors. It includes: (1) No late collision. (2) No excessive collision. (3) No TX FIFO under-run. (4) No lost carrier.
13	DISCRC	Disable the appended CRC field. This is a control bit. =1: disable the CRC appending. =0: enable the CRC appending on the TX packet. When the status is updated, this bit will be kept in the previous setting.
12-7	Rsvd	Reserved
6	TXFUR	FIFO Under-Run.
5	LATEC	Late Collision.
4	EXCEEDC	Exceed Collision.
3-0	COLCNT	Collision Counts.

2. DTLEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DTLEN										

Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DTLEN	The length of the transmitted packet.

3. DTBP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DTBP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTBP	TX Buffer Pointer. This is a 32-bit address pointer.

4. DTNP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DTNP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTNP	TX Next Descriptor Pointer. This is a 32-bit descriptor address pointer and DTNP0 is always 0. This field must be pointed to next descriptor start address or its start address.

Notes:

1. *The TX descriptor start address must be double-word alignment.*
2. *The TX data buffer start address can be any byte alignment address.*
3. *The transmitted data are less than 60 bytes when drivers are run.*

13.3 MCR0: MAC Control Register 0 (00h)

Register Offset: 00h
Register Name: MCR0: MAC Control Register 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULLD	TXEIE	Rsvd	XMTEN	Reserved		FCEN	AMCP	RXEIE	FBCP	PROM	ADRB	ALONG	ARUNT	RCV EN	ACRCER

Bit	Name	Attribute	Description
15	FULLD	R/W	Full Duplex. Set 1: Full duplex. Set 0: Half duplex (default).
14	TXEIE	R/W	TX Early Interrupt Enable. Set 1: The MAC will generate one TX early interrupt when data are transmitted over early interrupt threshold (see MCR1[7:6]). Set 0: The TX early interrupt will be disabled.
13	Rsvd	RO	Reserved
12	XMTEN	R/W	Transmission Enable
11-10	Rsvd	RO	Reserved
9	FCEN	R/W	Flow Control Function Enable. Set 1: will enable flow control. Set 0: will disable flow control.
8	AMCP	R/W	Accept Multicast Packet. Set 1: will enable hash table function. Set 0: will disable hash table function.
7	RXEIE	R/W	RX Early Interrupt Enable. Set 1: The MAC will generate one RX early interrupt when data are received over early interrupt threshold (see MCR1[7:6]). Set 0: The RX early interrupt will be disabled.
6	FBCP	R/W	Filter Broadcast Packet. Set 1: to filter broadcast packets. Set 0: to accept broadcast packets.
5	PROM	R/W	Promiscuous Mode. Set 1: The MAC will receive all packets without checking the MAC address. Set 0: The MAC will only receive the packet that hits the MAC address.
4	ADRB	R/W	Accept DRIBBLE packet. Set 1: Enable to accept dribble packets. Set 0: Disable.
3	ALONG	R/W	Accept Long packet. Set 1: Enable to accept long packets. Set 0: Disable.
2	ARUNT	R/W	Accept RUNT packet. Set 1: Enable to accept runt packets. The packets which length > 6 and < 64 will be accepted, but the packets which length >0 and < 6 will be rejected. Set 0: Disable to accept runt packets.
1	RCVEN	R/W	Receive Enable. Set 1: Enable the packet receive. Set 0: Disable the packet receive.
0	ACRCER	R/W	Accept CRC Error packet. Set 1: Enable. Set 0: Disable.

13.4 MCR1: MAC Control Register 1 (04h)

Register Offset: 04h
Register Name: MCR1: MAC Control Register 1
Reset Value : 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUCP	WIDX	Reserved				TPF	ECR	EITH[1:0]		MAXLEN[1:0]		0	0	LBM	MRST

Bit	Name	Attribute	Description
15	AUCP	R/W	Filter uni-cast packets by hash-table. Set 1: Enable. Set 0: Disable.
14	WIDX	R/W	Write the hash index number that was hit by hash-table. Set 1: Enable to write the HIDX[5:0] into the RX descriptor. Set 0: Disable this function.
13-10	Rsvd	RO	Reserved
9	TPF	RO	Trigger Pause Frame to be transmitted. If flow control (the FCEN bit in MCR0 [9]) is enabled, this bit will be set automatically when received descriptors unavailable happen. TPF refers to the XMTEN bit (MCR0 [12]). When the XMTEN bit is set, the pause frame can be sent.
8	ECR	R/W	Excessive Collision Retransmit times. 0: 16 times (default). 1: 32 times.
7-6	EITH[1:0]	R/W	Early Interrupt Threshold. 00: 1129 bytes (default). 01: 1257 bytes. 10: 1385 bytes. 11: 1513 bytes.
5-4	MAXLEN [1:0]	R/W	Maximum Packet Length Selector. Define the length of long packets. 01: 1518 bytes (default). 10: 1522 bytes. 11: 1534 bytes. 00: 1537 bytes.
3-2	Rsvd	R/O	Reserved
1	LBM	R/W	Loop-Back mode. 0: Normal mode (default). 1: MAC loop-back.
0	MRST	R/W	MAC Reset. Set 1 to reset the MAC. After resets, this bit will be cleared to 0.

13.5 MBCR: MAC Bus Control Register (08h)

Register Offset: 08h
Register Name: MBCR: MAC Bus Control Register
Reset Value : 1F1Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RHPT[4:0]					Reserved		RXFTH[1:0]		TXFTH[1:0]		FIFOTL[1:0]	

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12-8	RHPT[4:0]	R/W	SDRAM Bus Request High Priority Timer. When the MAC issues a bus request to the SDRAM arbiter, this timer will start to count down. After this timer is timeout, if the SDRAM arbiter is still not granted to the MAC, the SDRAM bus request will become high priority. Wait time = 1 ~15 host clocks. (Default=15 host clocks) RHPT = 0, disable this function.
7-6	Rsvd	RO	Reserved
5-4	RXFTH[1:0]	R/W	RX FIFO Data Threshold. The MAC receive machine starts to move the received data into the host memory when receiving data over the RX FIFO threshold. 00: 8 bytes. 01: 16 bytes (default). 10: 32 bytes. 11: 64 bytes.
3-2	TXFTH[1:0]	R/W	TX FIFO Data Threshold. The MAC transmit machine starts to send out packets to the PHY when data is transmitted into the TX FIFO over the threshold. 00: 16 bytes. 01: 32 bytes. 10: 64 bytes (default). 11: 96 bytes.
1-0	FIFOTL[1:0]	R/W	FIFO Transfer Length. Every transfer data length between the MAC FIFO and SDRAM. 00: 4 bytes. 01: 8 bytes. 10: 16 bytes (default). 11: 32 bytes.

Note: *This register is updated only when RCVEN=0.*

13.6 MTICR: MAC TX Interrupt Control Register (0Ch)

Register Offset: 0Ch
Register Name: MTICR: MAC TX Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXINTC[3:0]				Reserved		TXTIMER[5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	TXINTC[3:0]	R/W	TX Interrupt Control. 0: Turn off this function. N: An interrupt is generated after N packets (1~15 packets) are sent.
7-6	Rsvd	RO	Reserved
5-0	TXTIMER [5:0]	R/W	Wait TX Timer. When timeout, an interrupt is automatically generated. Timer waiting time: (63 + TXTIMER * 64) TX clock

13.7 MRICR: MAC RX Interrupt Control Register (10h)

Register Offset: 10h
Register Name: MRICR: MAC RX Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RXINTC[3:0]				Reserved		RXTIMER[5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	RXINTC[3:0]	R/W	RX Interrupt Control. 0: Turn off this function. N: An interrupt is generated after N packets (1~15 packets) are received.
7-6	Rsvd	RO	Reserved
5-0	RXTIMER [5:0]	R/W	Wait RX Timer. When timeout, an interrupt is automatically generated. Timer waiting time: (63 + RXTIMER * 64) RX clock

13.8 MTPR: MAC TX Poll Command Register (14h)

Register Offset: 14h
Register Name: MTPR: MAC TX Poll Command Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TM2TX

Bit	Name	Attribute	Description
15-1	Rsvd	RO	Reserved
0	TM2TX	R/W	Trigger the MAC to Transmit. When Write: Trigger the MAC to check the TX description owner bit. If the owner bit=0, the MAC will standby until the owner bit=1 to start transmission. When Read: TM2TX is current transmission status. When TM2TX= 1, it means the MAC is in transmitting. When TM2TX= 0, it means the transmission is complete.

13.9 MRBSR: MAC RX Buffer Size Register (18h)

Register Offset: 18h
Register Name: MRBSR: MAC RX Buffer Size Register
Reset Value : 0600h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RBSZ[10:0]									RBSZ[1:0]	

Note: *This register is updated onely when RCVEN=0.*

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10-2	RBSZ[10:2]	R/W	RX Buffer Size bit [10:2] for all RX frame data buffer of descriptors.
1-0	RBSZ[1:0]	R/W	RX Buffer Size bit [1:0] must be 00.

13.10 MRDCR: MAC RX Descriptor Control Register (1Ah)

Register Offset: 1Ah
Register Name: MRDCR: MAC RX Descriptor Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXPT[7:0]								RXDESPAN[7:0]							

Bit	Name	Attribute	Description
15-8	RXPT[7:0]	R/W	RX Descriptor Threshold value. The MAC controller will send TX Pause Frame when the available RX descriptor reaches this threshold value.
7-0	RXDESPAN [7:0]	R/W	RX Descriptor Available Number for flow-control. When the MAC finishes one descriptor data transfer into the RX buffer, the RX descriptor available number will decrease 1 automatically. Use the “IN” instruction to read this register and “OUT” instruction to increase the register value. When RCVEN=0, use the “OUT” instruction to setup the RX descriptor available number. When RCVEN=1, use the “OUT” instruction to increase the RX descriptor available number. This register must be initialized before RCVEN = 1.

13.11 MLSR: MAC Last Status Register (1Ch)

Register Offset: 1Ch
Register Name: MLSR: MAC Last Status Register
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFOR	LATEC	EXCEEDC	Reserved		RXDESPUA	TXFUR	Rsvd	PHYEER	DRIBBLE	OBL	LONG	RUNT	CRCERR	BROADCAST	MULTICAST

Bit	Name	Attribute	Description
15	RXFOR	RO	RX FIFO Over-Run.
14	LATEC	RO	Transmit Late Collision.
13	EXCEEDC	RO	Transmit Exceed Collision.
12-11	Rsvd	RO	Reserved.
10	RXDESPUA	RO	RX Descriptor Unavailable.
9	TXFUR	RO	TX FIFO Under-Run.
8	Rsvd	RO	Reserved.
7	PHYERR	RO	PHY RX Error.
6	DRIBBLE	RO	Dribble Packet.

5	OBL	RO	Received Packet Length Over Buffer Length.
4	LONG	RO	Received Packets Too Long.
3	RUNT	RO	Received Packets Too Short.
2	CRCERR	RO	Received Packets with CRC Errors.
1	BROADCAST	RO	Received Broadcast Packets.
0	MULTICAST	RO	Received Multicast Packets.

Note: *The MAC last time status is updated by next packet coming.*

13.12 MMDIO: MAC MDIO Control Register (20h)

Register Offset: 20h
Register Name: MMDIO: MAC MDIO Control Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	MIIWR	MIIRD	PHYAD[4:0]					Reserved			REGAD[4:0]				

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14	MIIWR	R/W	MDIO Write. Set 1 to write MIIWDATA [15:0] to the MDIO. It will be cleared after the operation is complete.
13	MIIRD	R/W	MDIO Read. Set 1 to read data from the MDIO into MIIRDATA [15:0]. It will be cleared after the operation is complete.
12-8	PHYAD[4:0]	R/W	PHY address.
7-5	Rsvd	RO	Reserved
4-0	REGAD[4:0]	R/W	REG address.

13.13 MMRD: MAC MDIO Read Data Register (24h)

Register Offset: 24h
Register Name: MMRD: MAC MDIO Read Data Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIRDATA[15:0]															

Bit	Name	Attribute	Description
15-0	MIIRDATA[15:0]	RO	MII Read Data. The data, read from the MDIO, are put in this register.

13.14 MMWD: MAC MDIO Write Data Register (28h)

Register Offset: 28h
Register Name: MMWD: MAC MDIO Write Data Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIWDATA[15:0]															

Bit	Name	Attribute	Description
15-0	MIIWDATA [15:0]	R/W	MII Write Data. The data, intended for being written to the MDIO, are put in this register.

13.15 MTDSA0: MAC TX Descriptor Start Address 0 (2Ch)

Register Offset: 2Ch
Register Name: MTDSA0: MAC TX Descriptor Start Address 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDSA[15:1]															0

Bit	Name	Attribute	Description
15-1	TDSA[15:1]	R/W	TX Descriptor Start Address bit[15:1] that are currently being sent.
0	0	RO	This bit must be 0.

Notes:
1. This register is initialized only when XMTEN=0.
2. The first TX descriptor start address TDSA[31:0] = {MTDSA1[15:0], MTDSA0[15:0]} must be double-word alignment. The MAC will update the TX descriptor start address when the previous TX is finished.

13.16 MTDSA1: MAC TX Descriptor Start Address 1 (30h)

Register Offset: 30h
Register Name: MTDSA1: MAC TX Descriptor Start Address 1
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDSA[31:16]															

Bit	Name	Attribute	Description
15-0	TDSA[31:16]	RW	TX Descriptor Start Address bit [31:16] that are currently being sent.

Note: *This register is initialized only when XMTEN=0.*

13.17 MRDSA0: MAC RX Descriptor Start Address 0 (34h)

Register Offset: 34h
Register Name: MRDSA0: MAC RX Descriptor Start Address 0
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDSA[15:1]															0

Bit	Name	Attribute	Description
15-1	RDSA[15:1]	R/W	RX Descriptor Start Address bit [15:1].
0	0	RO	This bit must be 0.

Notes:
1. This register is initialized only when RCVEN=0.
2. The first RX descriptor start address RDSA[31:0] = {MRDSA1[15:0], MRDSA0[15:0]} must be double-word alignment. The MAC will update the RX descriptor start address after the previous RX is finished.

13.18 MRDSA1: MAC RX Descriptor Start Address 1 (38h)

Register Offset: 38h
Register Name: MRDSA1: MAC RX Descriptor Start Address 1
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDSA[31:16]															

Bit	Name	Attribute	Description
15-0	RDSA[31:16]	RW	The first RX Descriptor Start Address bit [31:16].

Note: *This register is initialized only when RCVEN=0.*

13.19 MISR: MAC INT Status Register (3Ch)

Register Offset: 3Ch
Register Name: MISR: MAC INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PCHG	ECNTO	TXEI	Reserved		TXEND	RXEI	RXFF	RXDUA	RXEND

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	PCHG	RC	PHY Media Changed Interrupt status.
8	ECNTO	RC	Event Counter Overflow Interrupt status.
7	TXEI	RC	TX Early Interrupt status.
6-5	Rsvd	RO	Reserved.
4	TXEND	RC	Transmit Packet Finish Interrupt status.
3	RXEI	RC	RX Early Interrupt status.
2	RXFF	RC	RX FIFO Full Interrupt status.
1	RXDUA	RC	RX Descriptor Unavailable Interrupt status.
0	RXEND	RC	Receive Packet Finish Interrupt status.

Note: *RC = Read/Clear*

13.20 MIER: MAC INT Enable Register (40h)

Register Offset: 40h
Register Name: MIER: MAC INT Enable Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCHGE	ECNTOE	TXEIEN	Reserved		TXENDE	RXEIE	RXFFE	RXDNAE	RXENDE

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	MCHGE	RW	PHY Link Changed Interrupt Enable Set 1: Enable the MAC to generate interrupts to the CPU.
8	ECNTOE	R/W	Event Counter Overflow Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.
7	TXEIEN	R/W	TX Early Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.
6-5	Rsvd	RO	Reserved.
4	TXENDE	R/W	Transmit Packet Finish Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.

3	RXEIE	R/W	RX Early Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.
2	RXFFE	R/W	RX FIFO Full Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.
1	RXDNAE	R/W	RX Descriptor Unavailable Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.
0	RXENDE	R/W	Receive Packet Finish Interrupt Enable. Set 1: Enable the MAC to generate interrupts to the CPU.

13.21 MECISR: MAC Event Counter INT Status Register (44h)

Register Offset: 44h

Register Name: MECISR: MAC Event Counter INT Status Register

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCI	LCCI	STPCI	RFFCI	RDUCI	Rsvd	LONGCI	RUNTCI	CRCECI	BCCI	MCCI	SRPCI

The correspond bit in the Event Counter INT Status Register will be set when the MSB bit in the related Event Counter register is set to 1. Reading the Event Counter register will clear the corresponding bits. Those event counters will keep increasing until reaching 255 or 65535.

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCI	RO	TX FIFO under-run Dropped Packet Counter Interrupt status.
10	LCCI	RO	TX Late Collision Counter Interrupt status.
9	STPCI	RO	TX Successfully Package Counter Interrupt status.
8	RFFCI	RO	RX FIFO Full Counter Interrupt status.
7	RDUCI	RO	RX Descriptor Unavailable Dropped Packet Counter Interrupt status.
6	Rsvd	RO	Reserved.
5	LONGCI	RO	RX Long Packet Counter Interrupt status.
4	RUNTCI	RO	RX Runt Packet Counter Interrupt status.
3	CRCECI	RO	RX CRC Error Packet Counter Interrupt status.
2	BCCI	RO	RX Broadcast Packet Counter Interrupt status.
1	MCCI	RO	RX Multicast Packet Counter Interrupt status.
0	SRPCI	RO	RX Successfully Packet Counter Interrupt status.

13.22 MECIER: MAC Event Counter INT Enable Register (48h)

Register Offset: 48h
Register Name: MECIER: MAC Event Counter INT Enable Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCIE	LCCIE	STPCIE	RFFCIE	RDUCIE	Rsvd	LONGCIE	RUNTCIE	CRCECIE	BCCIE	MCCIE	SRPCIE

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCIE	RW	TX FIFO under-run Dropped Packet Counter Interrupt Enable
10	LCCIE	R/W	TX Late Collision Counter Interrupt Enable.
9	STPCIE	R/W	TX Successfully Packet Counter Interrupt Enable.
8	RFFCIE	R/W	RX FIFO Full Counter Interrupt Enable.
7	RDUCIE	R/W	RX Descriptor Unavailable Dropped Packet Counter Interrupt Enable.
6	Rsvd	RO	Reserved.
5	LONGCIE	R/W	RX Long Packet Counter Interrupt Enable.
4	RUNTCIE	R/W	RX Runt Packet Counter Interrupt Enable.
3	CRCECIE	R/W	RX CRC Error Packet Counter Interrupt Enable.
2	BCCIE	R/W	RX Broadcast Packet Counter Interrupt Enable.
1	MCCIE	R/W	RX Multicast Packet Counter Interrupt Enable.
0	SRPCIE	R/W	RX Successfully Packet Counter Interrupt Enable.

Note: *Reading any one of all the following event counter registers will clear its value to 0.*

13.23 MRCNT: MAC Successfully Received Packet Counter Register (50h)

Register Offset: 50h
Register Name: MRCNT: MAC Successfully Received Packet Counter Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRPCNT[15:0]															

Bit	Name	Attribute	Description
15-0	SRPCNT[15:0]	RC	Successfully Received Packet Counter

Note: *RC = Read/Clear*

13.24 MECNT0: MAC Event Counter 0 Register (52h)

Register Offset: 52h
Register Name: MECNT0: MAC Event Counter 0 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCCNT[7:0]								MCCNT[7:0]							

Bit	Name	Attribute	Description
15-8	BCCNT[7:0]	RC	Receive Broadcast Packet Counter.
7-0	MCCNT[7:0]	RC	Receive Multicast Packet Counter.

Note: *RC = Read/Clear*

13.25 MECNT1: MAC Event Counter 1 Register (54h)

Register Offset: 54h
Register Name: MECNT1: MAC Event Counter 1 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUNCNT[7:0]								CRCECNT[7:0]							

Bit	Name	Attribute	Description
15-8	RUNCNT[7:0]	RC	Receive Run Packet Counter.
7-0	CRCECNT[7:0]	RC	Receive CRC Error Packet Counter.

Note: *RC = Read/Clear*

13.26 MECNT2: MAC Event Counter 2 Register (56h)

Register Offset: 56h
Register Name: MECNT2: MAC Event Counter 2 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								LONGCNT[7:0]							

Bit	Name	Attribute	Description
15-8	Rsvd	RC	Reserved
7-0	LONGCNT[7:0]	RC	Receive Long Packet Counter.

Note: *RC = Read/Clear*

13.27 MCENT3: MAC Event Counter 3 Register (58h)

Register Offset: 58h
Register Name: MECNT3: MAC Event Counter 3 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFFCNT[7:0]								RDUVCNT[7:0]							

Bit	Name	Attribute	Description
15-8	RFFCNT[7:0]	RC	RX FIFO Full Packet Counter.
7-0	RDUVCNT[7:0]	RC	RX Descriptor Unavailable Packet lost Counter.

Note: *RC = Read/Clear*

13.28 MTCNT: MAC Successfully Transmit Packet Counter Register (5Ah)

Register Offset: 5Ah
Register Name: MTCNT: MAC Successfully Transmit Packet Counter Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STPCNT[15:0]															

Bit	Name	Attribute	Description
15-0	STPCNT[15:0]	RC	Successfully Transmitted Packet Counter.

Note: *RC = Read/Clear*

13.29 MCENT4: MAC Event Counter 4 Register (5Ch)

Register Offset: 5Ch
Register Name: MECNT4: MAC Event Counter 4 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDPCNT[7:0]								LCCNT[7:0]							

Bit	Name	Attribute	Description
15-8	TDPCNT[7:0]	RC	TX Dropped Packet Counter by TX FIFO under-run.
7-0	LCCNT[7:0]	RC	TX Late Collision Packet Counter.

Note: *RC = Read/Clear*

13.30 MPCNT: MAC Pause Frame Counter Register (5Eh)

Register Offset: 5Eh
Register Name: MPCNT: MAC Pause Frame Counter Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXPFCNT[7:0]								RXPFCNT[7:0]							

Bit	Name	Attribute	Description
15-8	TXPFCNT[7:0]	RC	Transmitted Pause Frame Counter.
7-0	RXPFCNT[7:0]	RC	Received Pause Frame Counter.

Note: *RC = Read/Clear*

13.31 MAR0 ~3: MAC Hash Table Word 0 ~3 (60h, 62h, 64h, 66h)

Register Offset: 60h
Register Name: MAR0: MAC Hash Table Word 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR0[15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR0[15:0]	R/W	Hash Table Word 0.

Register Offset: 62h
Register Name: MAR1: MAC Hash Table Word 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR1[15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR1[15:0]	R/W	Hash Table Word 1.

Register Offset: 64h
Register Name: MAR2: MAC Hash Table Word 2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR2[15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR2[15:0]	R/W	Hash Table Word 2.

Register Offset: 66h
Register Name: MAR3: MAC Hash Table Word 3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR3[15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR3[15:0]	R/W	Hash Table Word 3.

13.32 MID0 (68h, 6Ah, 6Ch)

Register Offset: 68h
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0L[15:0]															

Register Offset: 6Ah
Register Name: MID0
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0M[15:0]															

Register Offset: 6Ch
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0H[15:0]															

The MAC/Multicast address MID0[47:0] = {MID0H[15:0], MID0M[15:0], MID0L[15:0]};
For example: The MAC address is 01:02:03:04:05:06; the contents for MID are:
MID0L[15:0] = 0201h
MID0M[15:0] = 0403h
MID0H[15:0] = 0605h

Bit 15-0: MID0L[15:0], the two bytes in the first line of the MAC/Multicast address.
Bit 15-0: MID0M[15:0], the two bytes in the second line of the MAC/Multicast address.
Bit 15-0: MID0H[15:0], the two bytes in the last line of the MAC/Multicast address.

13.33 MID1 (70h, 72h, 74h)

Register Offset: 70h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1L[15:0]															

Register Offset: 72h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1M[15:0]															

Register Offset: 74h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1H[15:0]															

The MAC/Multicast address MID1[47:0] = {MID1H[15:0], MID1M[15:0], MID1L[15:0]};
Bit 15-0: MID1L[15:0], the two bytes in the first line of the MAC/Multicast address.
Bit 15-0: MID1M[15:0], the two bytes in the second line of the MAC/Multicast address.
Bit 15-0: MID1H[15:0], the two bytes in the last line of the MAC/Multicast address.

13.34 MID2 (78h, 7Ah, 7Ch)

Register Offset: 78h
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2L[15:0]															

Register Offset: 7Ah
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2M[15:0]															

Register Offset: 7Ch
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2H[15:0]															

The MAC/Multicast address MID2[47:0] = {MID2H[15:0], MID2M[15:0], MID2L[15:0]};
Bit 15-0: MID2L[15:0], the two bytes in the first line of the MAC/Multicast address.
Bit 15-0: MID2M[15:0], the two bytes in the second line of the MAC/Multicast address.
Bit 15-0: MID2H[15:0], the two bytes in the last line of the MAC/Multicast address.

13.35 MID3 (80h, 82h, 84h)

Register Offset: 80h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3L[15:0]															

Register Offset: 82h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3M[15:0]															

Register Offset: 84h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3H[15:0]															

The MAC/Multicast address MID3[47:0] = {MID3H[15:0], MID3M[15:0], MID3L[15:0]};
Bit 15-0: MID3L[15:0], the two bytes in the first line of the MAC/Multicast address.
Bit 15-0: MID3M[15:0], the two bytes in the second line of the MAC/Multicast address.
Bit 15-0: MID3H[15:0], the two bytes in the last line of the MAC/Multicast address.

13.36 MPSCCR: MAC PHY Status Change Configuration Register (88h)

Register Offset: 88h
Register Name: MPSCCR: MAC PHY Status Change Configuration Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	Reserved			PHYAD[4:0]				Reserved					TMRDIV[2:0]		

Bit	Name	Attribute	Description
15	EN	R/W	PHY Status Change Enable
12-8	PHYAD[4:0]	R/W	PHY Address
7-3	Rsvd	RO	Reserved
2-0	TMRDIV[2:0]	R/W	Timer Divider The timer will time-out every host-clock*160*$2^{(16-TMRDIV)}$. If both PHY status change functions in MAC0 and MAC1 are enabled, the value of TMRDIV[2:0] belonged to MAC0 and MAC1 must be set alike.

13.37 MPSR: MAC PHY Status Register (8Ah)

Register Offset: 8Ah
Register Name: MPSR: MAC PHY Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPSR[15:0]															

Bit	Name	Attribute	Description
15-0	MPSR	RO	PHY Status Register

13.38 MACID: MAC Identifier Register

Register Offset: BEh
Register Name: MACID: MAC Identifier Register
Reset Value : 6040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC ID															

Bit	Name	Attribute	Description
15-0	MAC ID	RO	This register contains a 16-bit value assigned to the R3210 MAC.

14. DC Electrical Characteristics

14.1 Absolute Maximum Ratings (25℃)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC_CORE	Core Supply Voltage	1.71	1.89	V	
VCC18A	PLL Supply Voltage	1.71	1.89	V	
VCC_IO	I/O Supply Voltage	3.0	3.6	V	
AVDD [0:1]	Analog Suply Voltage	1.71	1.89	V	
AVDD33	I/O Supply Voltage	3.0	3.6	V	
AVDDPLL	USB PLL Supply Voltage	1.71	1.89	V	
Vil	Input Low Voltage	--	0.8	V	
Vih	Input High Voltage	2.0	--	V	
Vol	Output Low Voltage	--	0.4	V	
Voh	Output High Voltage	2.4	--	V	
Iin	Input leakage current	-10	10	uA	
Ioz	Tri-State output leakage current	-10	10	uA	

14.2 Temperature

Symbol	Parameter	Typ.	Unit	Conditions
T_{cop}	Case Surface Operating Temperature (case top)	43~49	℃	1. Ambient Temperature = 25℃ 2. Open case testing. 3. Note 2.
T_A	Ambient Operating Temperature	0~70	℃	Temperature of the surrounding medium
T_{stg}	Storage Temperature	-65~125	℃	Dry Pack.

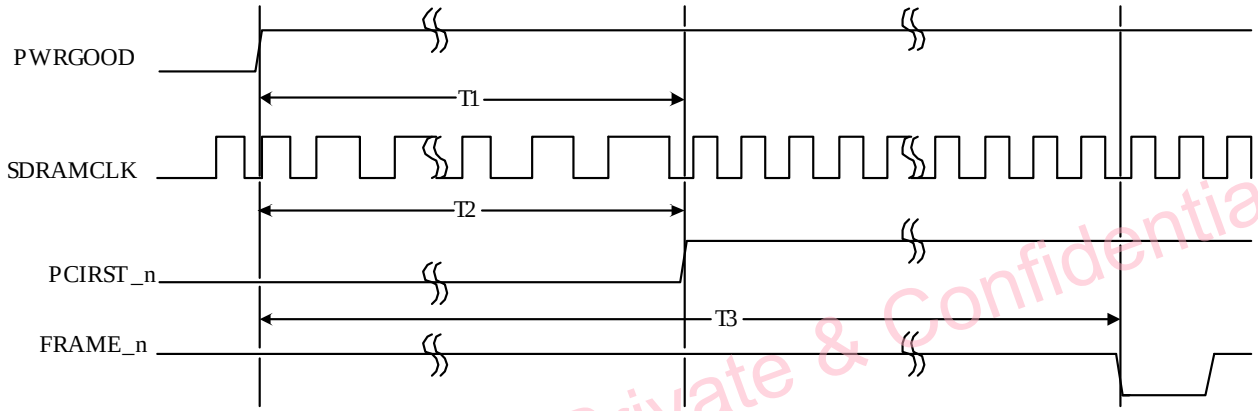
Notes:

1. *The IC should be mounted on PCB within 7 days after the dry pack is opened. If the IC is out of dry pack more than 7 days, it should be burned in oven (+125°C, > 12 hours) before mounted on PCB.*
2. *T_{cop} depends on the number of PCB layers, PCB size, system loading, working voltage and running pattern. The condition is for 4-layer A4-size PCB at typical working voltage.*

15. AC Electrical Characteristics

15.1 System Reset

Symbol	Parameter	Min.	Max.	Unit	Notes
T1	PWRGOOD active to SDRAMCLK output stable	1		ms	
T2	PWRGOOD active to PCIRST_n ready	1		ms	
T3	PWRGOOD active to first code fetch command	2		ms	

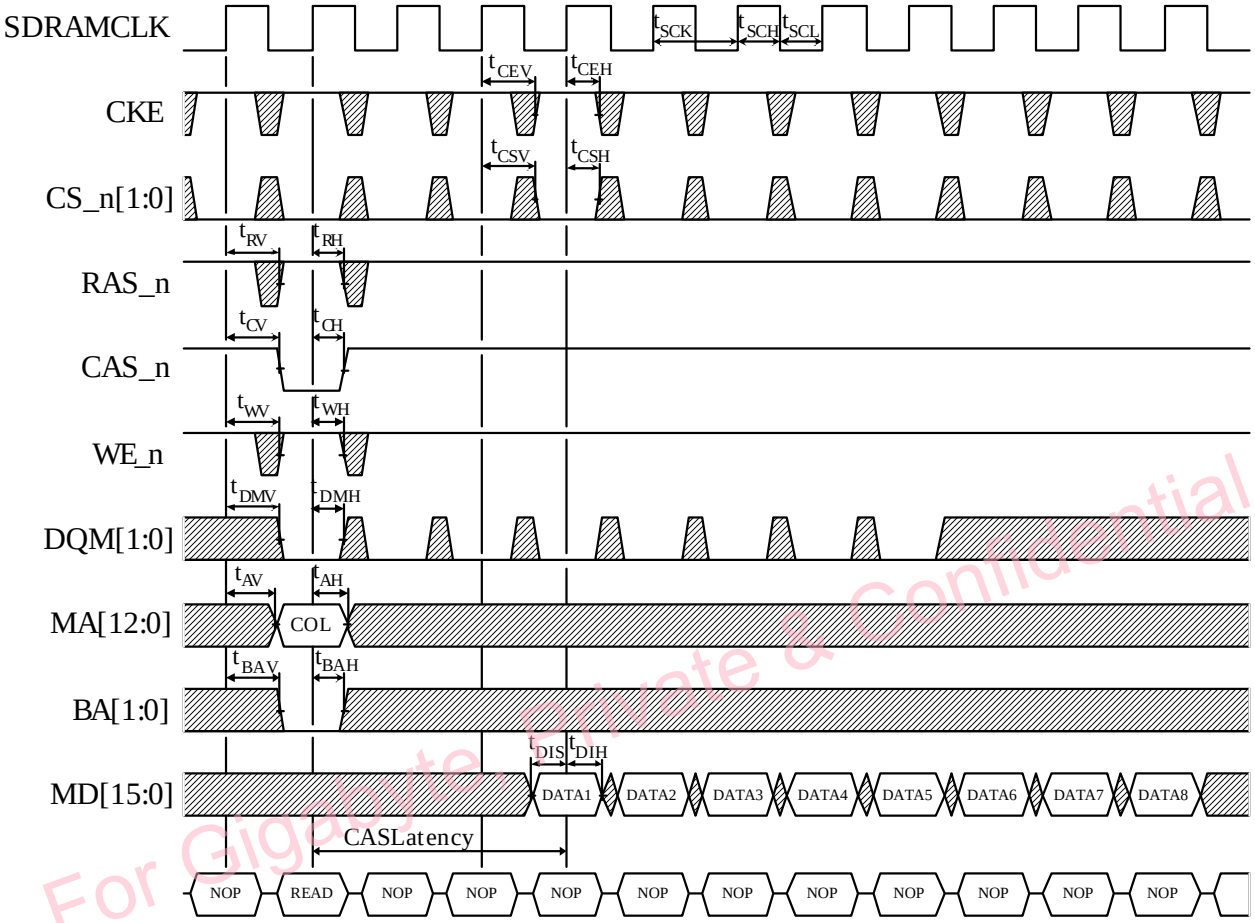


15.2 SDRAM Interface

- **Read Cycle (66MHz)**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tSCK	SDRAM clock cycle time	15.16	--	--	
tSCH	SDRAM clock high-level width	--	7.58	--	
tSCL	SDRAM clock low-level width	--	7.58	--	
tCEV	CKE valid delay time	--	--	6	
tCEH	CKE hold time	4	--	--	
tCSV	CS_n valid delay time	--	--	6	
tCSH	CS_n hold time	4	--	--	
tRV	RAS_n valid delay time	--	--	6	
tRH	RAS_n hold time	4	--	--	
tCV	CAS_n valid delay time	--	--	6	
tCH	CAS_n hold time	4	--	--	
tWV	WE_n valid delay time	--	--	6	
tWH	WE_n hold time	4	--	--	
tDMV	DQM valid delay time	--	--	6	
tDMH	DQM hold time	4	--	--	
tAV	Address valid delay time	--	--	5	
tAH	Address hold time	4	--	--	
tBAV	Bank address valid delay time	--	--	5	
tBAH	Bank address hold time	4	--	--	
tDIS	Data input setup time	2	--	--	
tDIH	Data input hold time	1	--	--	

- **Read Cycle Waveforms (I)**

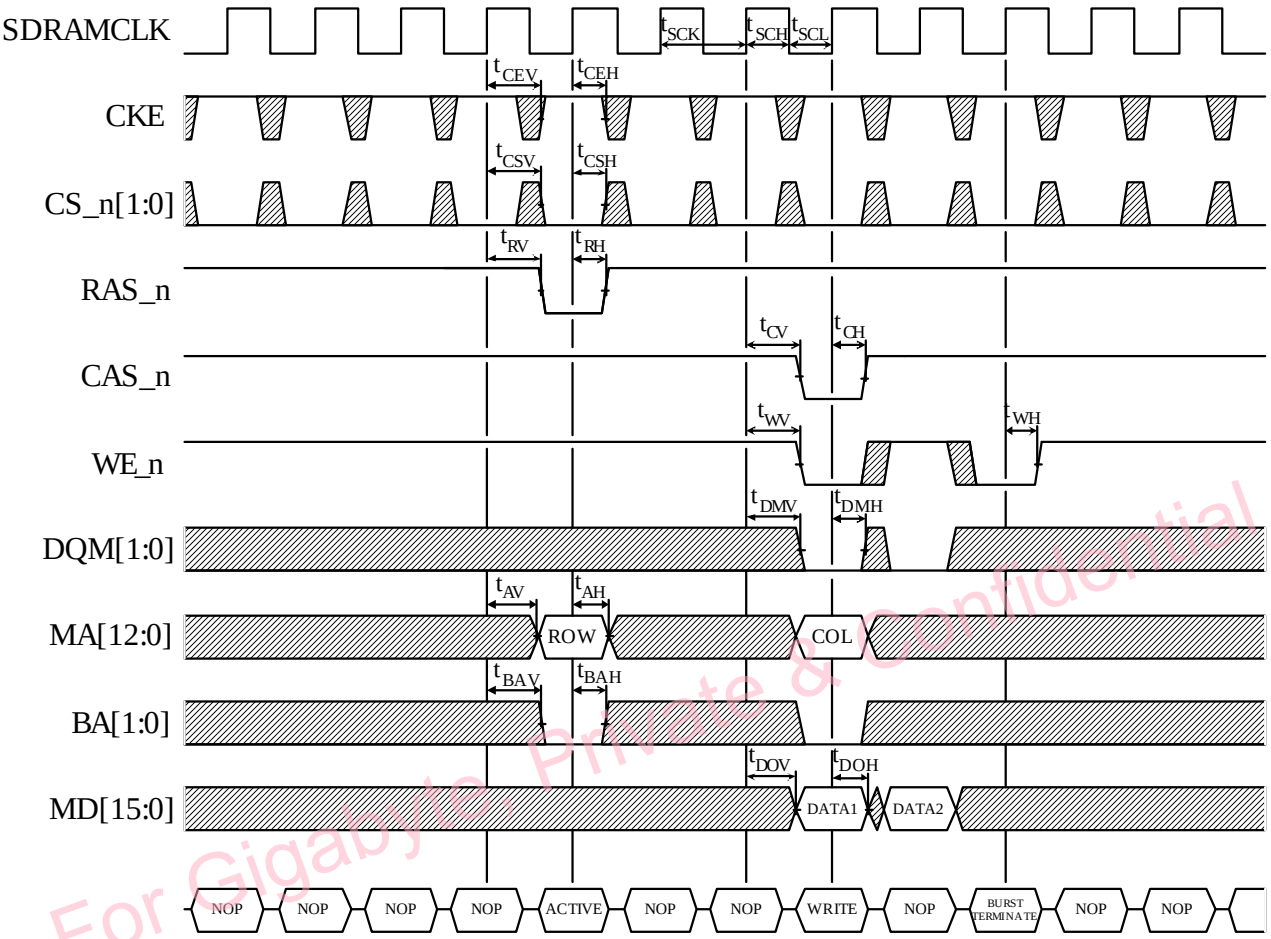


16-Bit Data Bus Burst Read Cycle

- **Write Cycle (66MHz)**

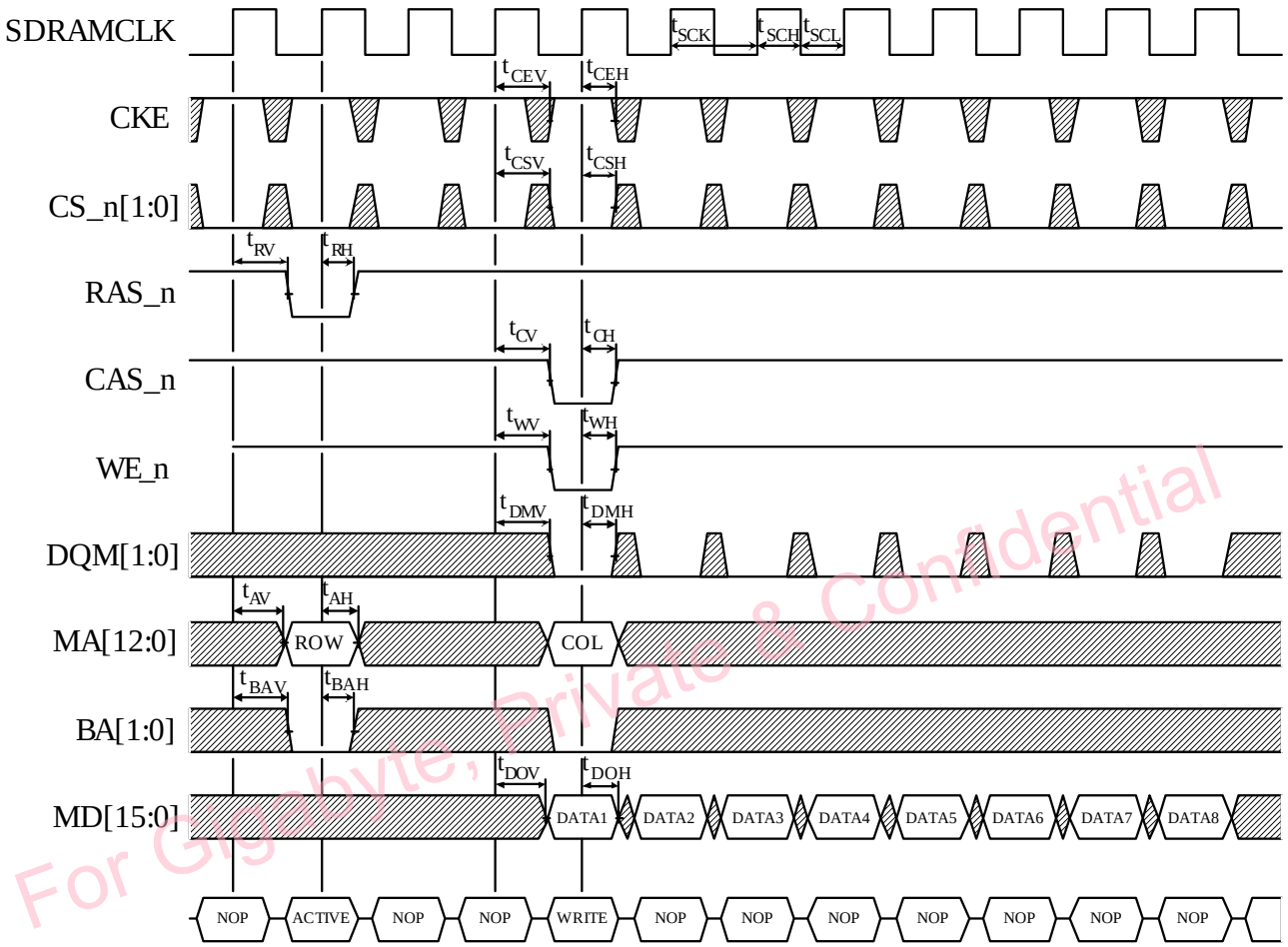
Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tSCK	SDRAM clock cycle time	15.16	--	--	
tSCH	SDRAM clock high-level width	--	7.58	--	
tSCL	SDRAM clock low-level width	--	7.58	--	
tCEV	CKE valid delay time	--	--	6	
tCEH	CKE hold time	4	--	--	
tCSV	CS_n valid delay time	--	--	6	
tCSH	CS_n hold time	4	--	--	
tRV	RAS_n valid delay time	--	--	6	
tRH	RAS_n hold time	4	--	--	
tCV	CAS_n valid delay time	--	--	6	
tCH	CAS_n hold time	4	--	--	
tWV	WE_n valid delay time	--	--	6	
tWH	WE_n hold time	4	--	--	
tDMV	DQM valid delay time	--	--	6	
tDMH	DQM hold time	4	--	--	
tAV	Address valid delay time	--	--	5	
tAH	Address hold time	4	--	--	
tBAV	Bank address valid delay time	--	--	5	
tBAH	Bank address hold time	4	--	--	
tDOV	Data output valid delay time	--	--	8	
tDOH	Data output hold time	2	--	--	

- **Write Cycle Waveforms (I)**



16-Bit Data Bus Write with Terminate

- **Write Cycle Waveforms (II)**



16-Bit Data Bus Burst Write Cycle

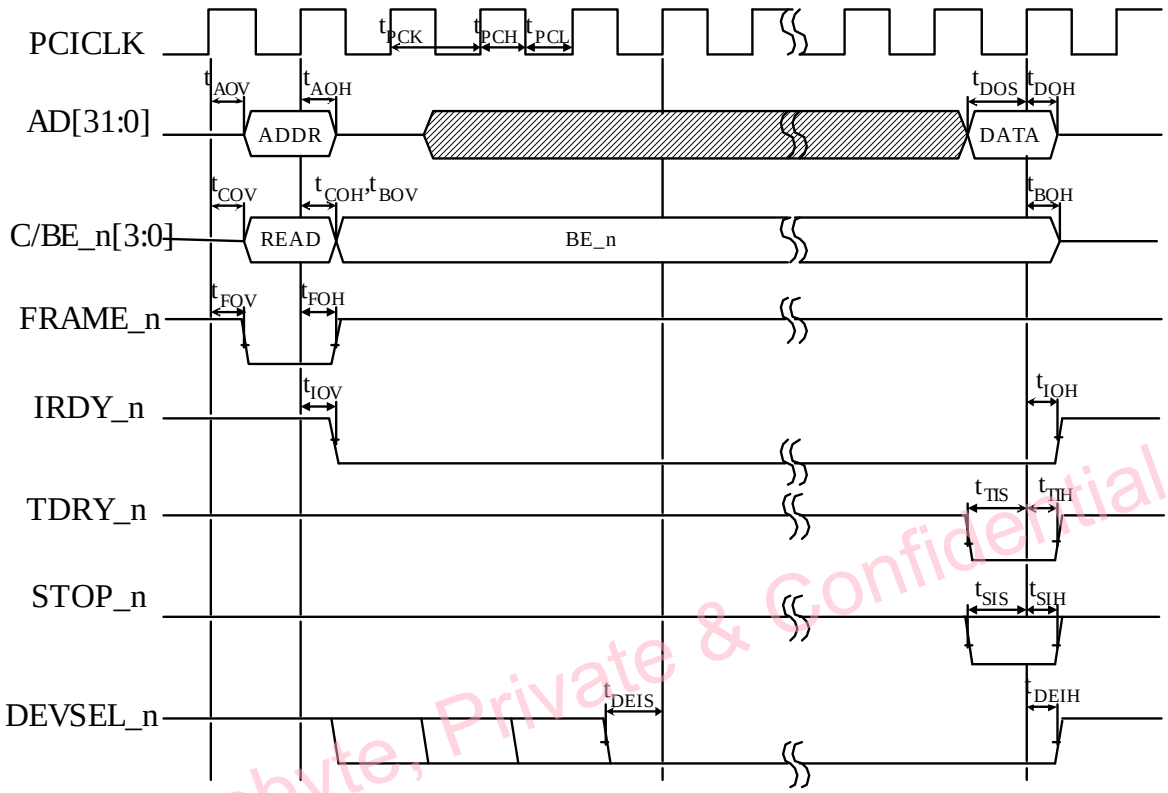
15.3 PCI Interface

15.3.1 R3210 as a PCI Master

- **Read Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	--	--	
tPCH	PCI clock high-level width	--	15	--	
tPCL	PCI clock low-level width	--	15	--	
tAOV	Address output valid delay time	2	--	11	
tAOH	Address output hold time	1	--	--	
tDOS	Data input setup time	7	--	--	
tDOH	Data input hold time	1	--	--	
tCOV	Command output valid delay time	2	--	11	
tCOH	Command output hold time	1	--	--	
tBOV	Byte Enable output valid delay time	2	--	11	
tBOH	Byte Enable output hold time	1	--	--	
tFOV	FRAME_n output valid delay time	2	--	11	
tFOH	FRAME_n output hold time	1	--	--	
tIOV	IRDY_n output valid delay time	2	--	11	
tIOH	IRDY_n output hold time	1	--	--	
tTIS	TRDY_n input setup time	7	--	--	
tTIH	TRDY_n input hold time	1	--	--	
tSIS	STOP_n input setup time	7	--	--	
tSIH	STOP_n input hold time	1	--	--	
tDEIS	DEVSEL_n input setup time	7	--	--	
tDEIH	DEVSEL_n input hold time	1	--	--	

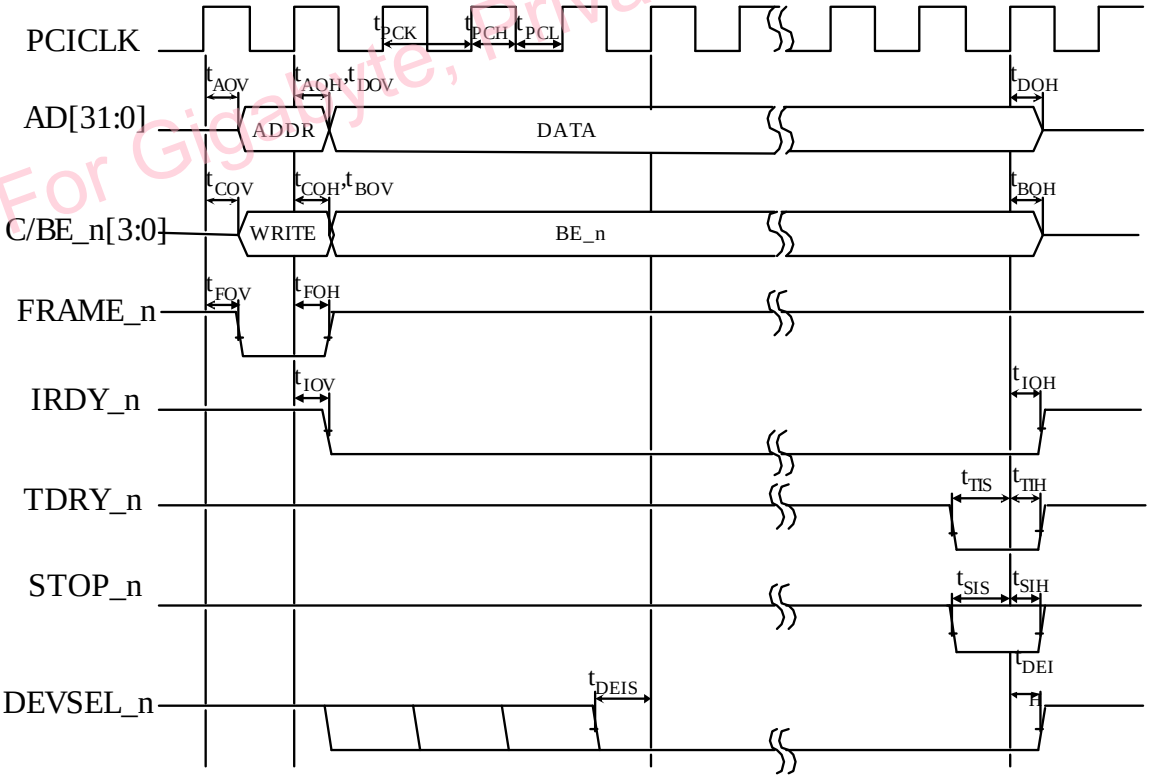
- **Memory Read Cycle Waveforms**



- **Write Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	--	--	
tPCH	PCI clock high-level width	--	15	--	
tPCL	PCI clock low-level width	--	15	--	
tAOV	Address output valid delay time	2	--	11	
tAOH	Address output hold time	1	--	--	
tDOV	Data output valid delay time	2	--	11	
tDOH	Data output hold time	1	--	--	
tCOV	Command output valid delay time	2	--	11	
tCOH	Command output hold time	1	--	--	
tBOV	Byte Enable output valid delay time	2	--	11	
tBOH	Byte Enable output hold time	1	--	--	
tFOV	FRAME_n output valid delay time	2	--	11	
tFOH	FRAME_n output hold time	1	--	--	
tIOV	IRDY_n output valid delay time	2	--	11	
tIOH	IRDY_n output hold time	1	--	--	
tTIS	TRDY_n input setup time	7	--	--	
tTIH	TRDY_n input hold time	1	--	--	
tSIS	STOP_n input setup time	7	--	--	
tSIH	STOP_n input hold time	1	--	--	
tDEIS	DEVSEL_n input setup time	7	--	--	
tDEIH	DEVSEL_n input hold time	1	--	--	

- **Memory Write Cycle Waveforms**

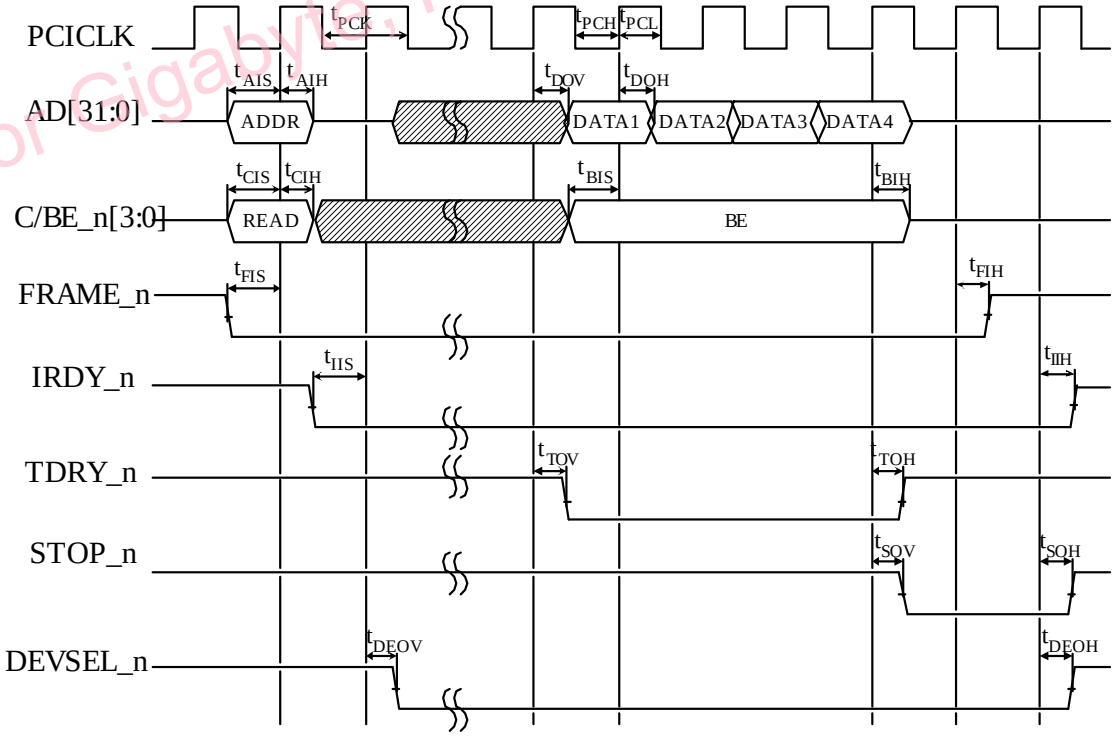


15.3.2 R3210 as a PCI Target

- **Read Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	--	--	
tPCH	PCI clock high-level width	--	15	--	
tPCL	PCI clock low-level width	--	15	--	
tAIS	Address input setup time	7	--	--	
tAIH	Address output hold time	1	--	--	
tDOV	Data output valid delay time	2	--	11	
tDOH	Data output hold time	1	--	--	
tCIS	Command input setup time	7	--	--	
tCIH	Command input hold time	1	--	--	
tBIS	Byte Enable input setup time	7	--	--	
tBIH	Byte Enable input hold time	1	--	--	
tFIS	FRAME_n input setup time	7	--	--	
tFIH	FRAME_n input hold time	1	--	--	
tIIS	IRDY_n input setup time	7	--	--	
tIIH	IRDY_n input hold time	1	--	--	
tTOV	TRDY_n output valid delay time	2	--	11	
tTOH	TRDY_n output hold time	1	--	--	
tSOV	STOP_n output valid delay time	2	--	11	
tSOH	STOP_n output hold time	1	--	--	
tDEOV	DEVSEL_n output valid delay time	2	--	11	
tDEOH	DEVSEL_n output hold time	1	--	--	

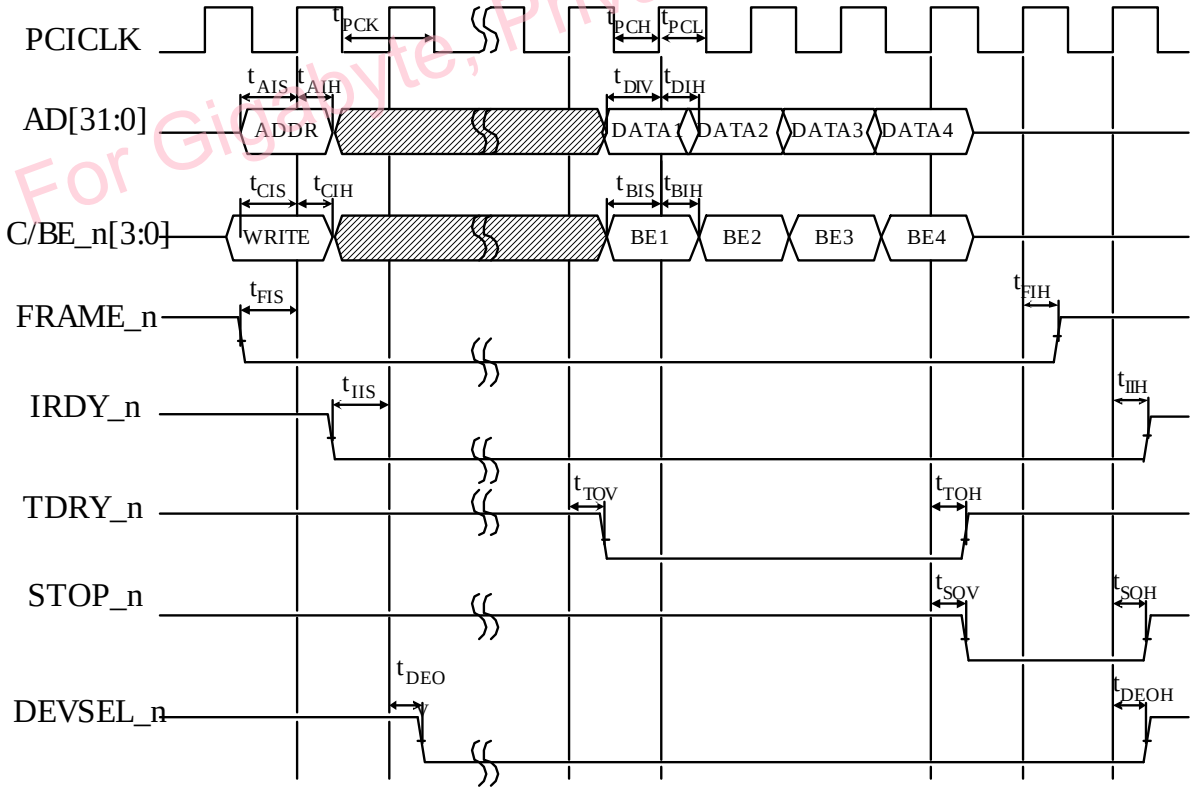
- **Burst Read Cycle Waveforms**



- **Write Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	--	--	
tPCH	PCI clock high-level width	--	15	--	
tPCL	PCI clock low-level width	--	15	--	
tAIS	Address input setup time	7	--	--	
tAIH	Address output hold time	1	--	--	
tDIV	Data input setup time	7	--	--	
tDIH	Data input hold time	1	--	--	
tCIS	Command input setup time	7	--	--	
tCIH	Command input hold time	1	--	--	
tBIS	Byte Enable input setup time	7	--	--	
tBIH	Byte Enable input hold time	1	--	--	
tFIS	FRAME_n input setup time	7	--	--	
tFIH	FRAME_n input hold time	1	--	--	
tIIS	IRDY_n input setup time	7	--	--	
tIIH	IRDY_n input hold time	1	--	--	
tTOV	TRDY_n output valid delay time	2	--	11	
tTOH	TRDY_n output hold time	1	--	--	
tSOV	STOP_n output valid delay time	2	--	11	
tSOH	STOP_n output hold time	1	--	--	
tDEOV	DEVSEL_n output valid delay time	2	--	11	
tDEOH	DEVSEL_n output hold time	1	--	--	

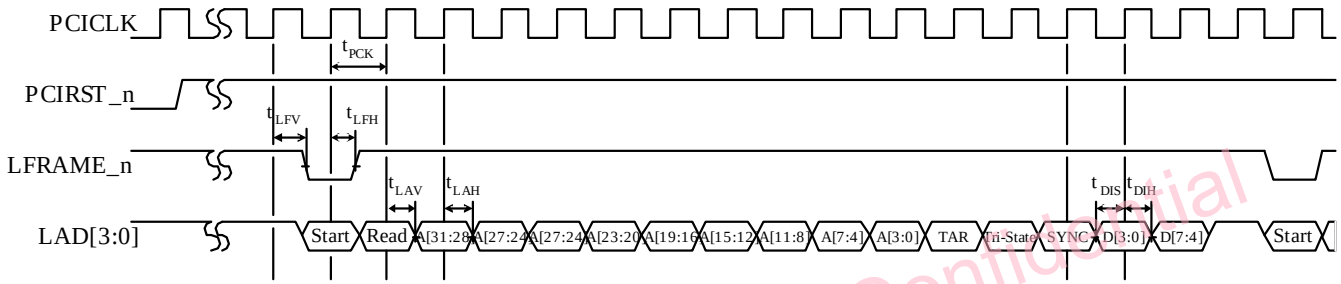
- **Burst Write with Disconnect without Data**



15.4 LPC Interface

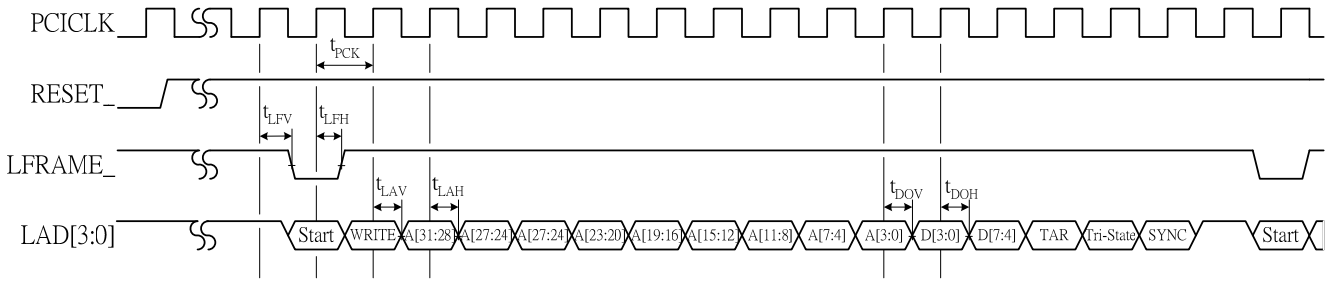
- **Memory Read Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	--	--	
tLFV	LFRAM_n valid delay time	--	--	23	
tLFH	LFRAM_n hold time	2	--	--	
tLAV	Address valid delay time	--	--	23	
tLAH	Address hold time	2	--	--	
tDIS	Data input setup time	7	--	--	
tDIH	Data input hold time	2	--	--	



- **Memory Write Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	--	--	
tLFV	LFRAM_n valid delay time	--	--	23	
tLFH	LFRAM_n hold time	2	--	--	
tLAV	Address valid delay time	--	--	23	
tLAH	Address hold time	2	--	--	
tDOV	Data output valid delay time	--	--	23	
tDOH	Data output hold time	2	--	--	

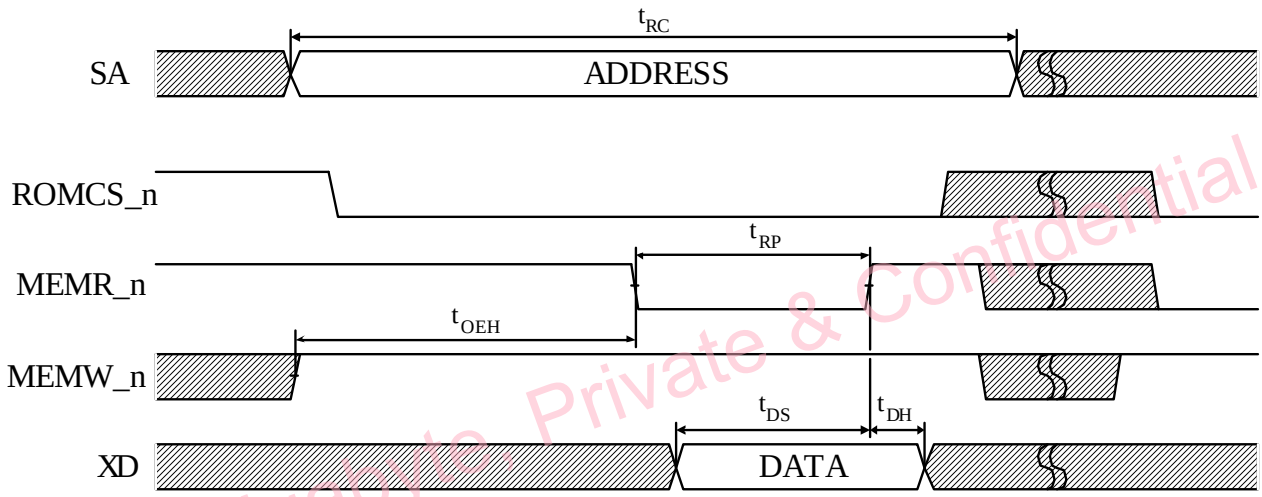


15.5 Bus Interface

- **Read Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tRC	Read cycle time		500		
tOEH	MEMR_n hold time		500		
tRP	MEMR_n pulse width		240		
tDS	Data setup time		10		
tDH	Data hold time		0		

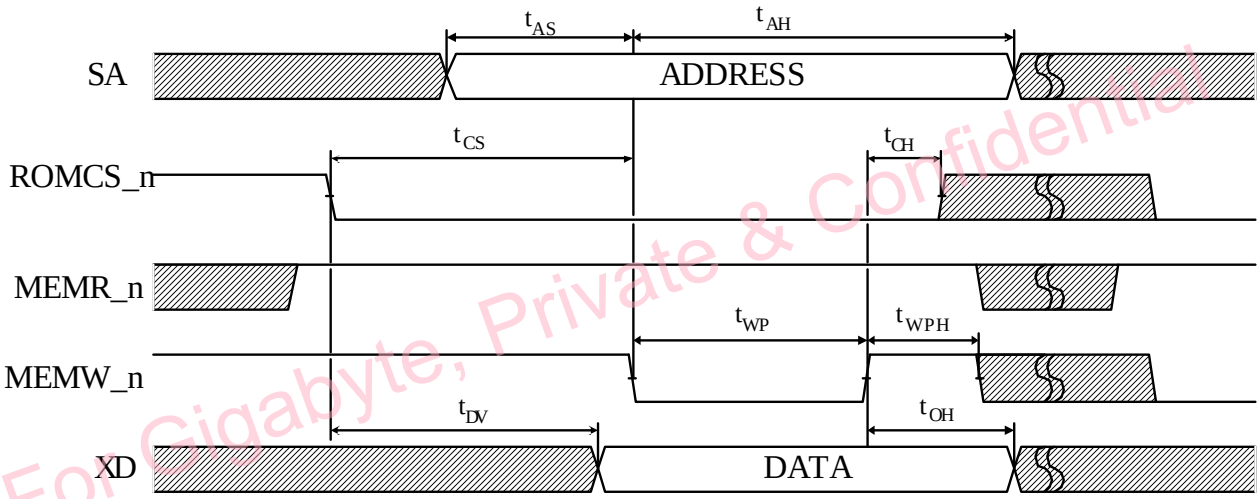
- **Read Cycle Waveforms**



- **Write Cycle**

Symbol	Parameter	Min. (ns)	Type (ns)	Max. (ns)	Notes
tAS	Address setup time		208		
tAH	Address hold time		360		
tCS	MEMW_n & ROMCS_n setup time		178		
tCH	MEMW_n & ROMCS_n hold time		62		
tWP	MEMW_n pulse width		240		
tWPH	MEMW_n high width		240		
tDV	Data valid time		180		
tDH	Data hold time		120		

- **Write Cycle Waveforms**



16. Package Information

LQFP: 216 pins

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D_1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E_1	23.90	24.00	24.10	0.941	0.945	0.949
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 REF			0.039 REF	
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°