

Hi3536-10HDD V1.0

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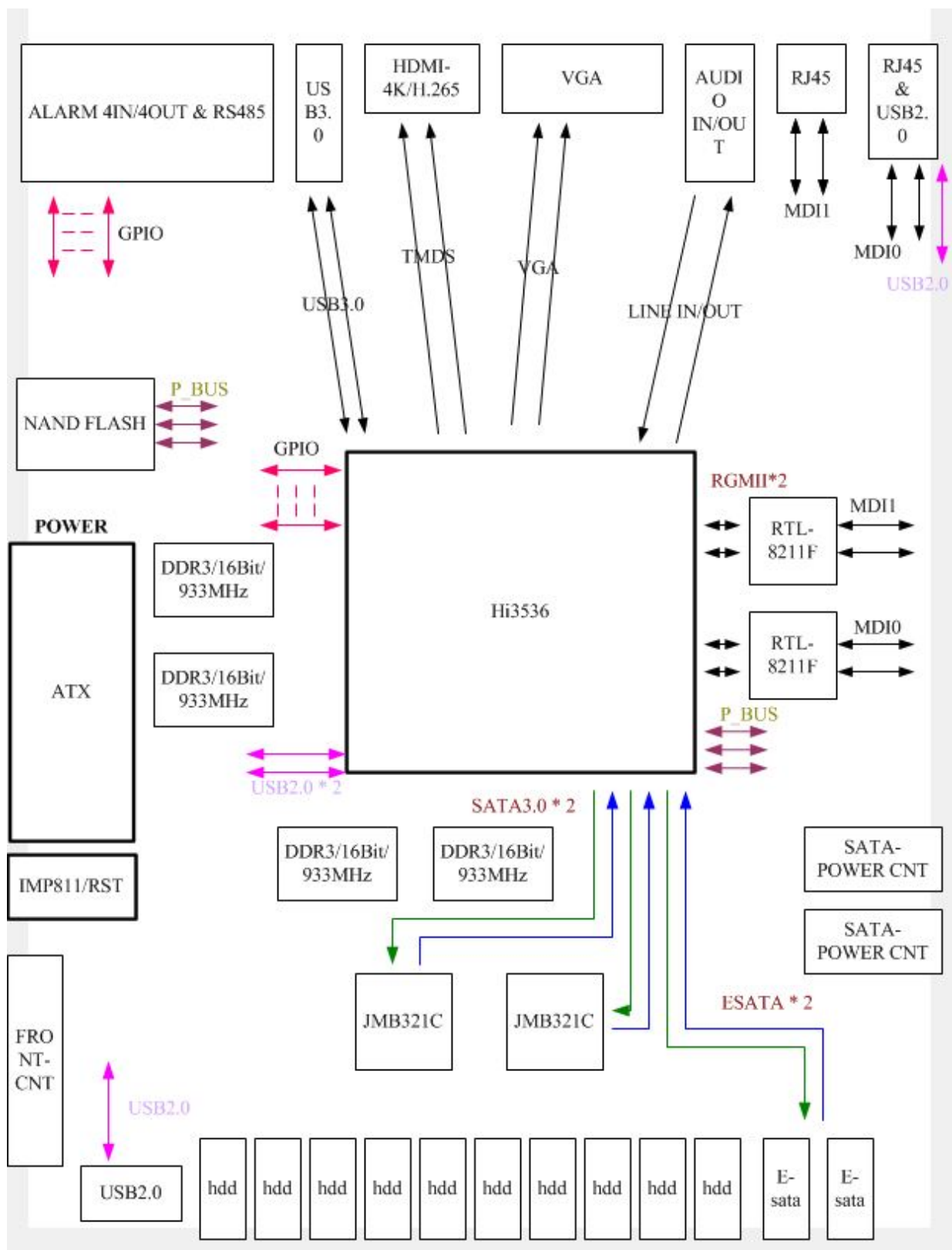
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Title H3536-10HDD Design By ANTS HW		
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CHANGE LIST

2015.03.24 V1.0

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BLOCK DIAGRAM

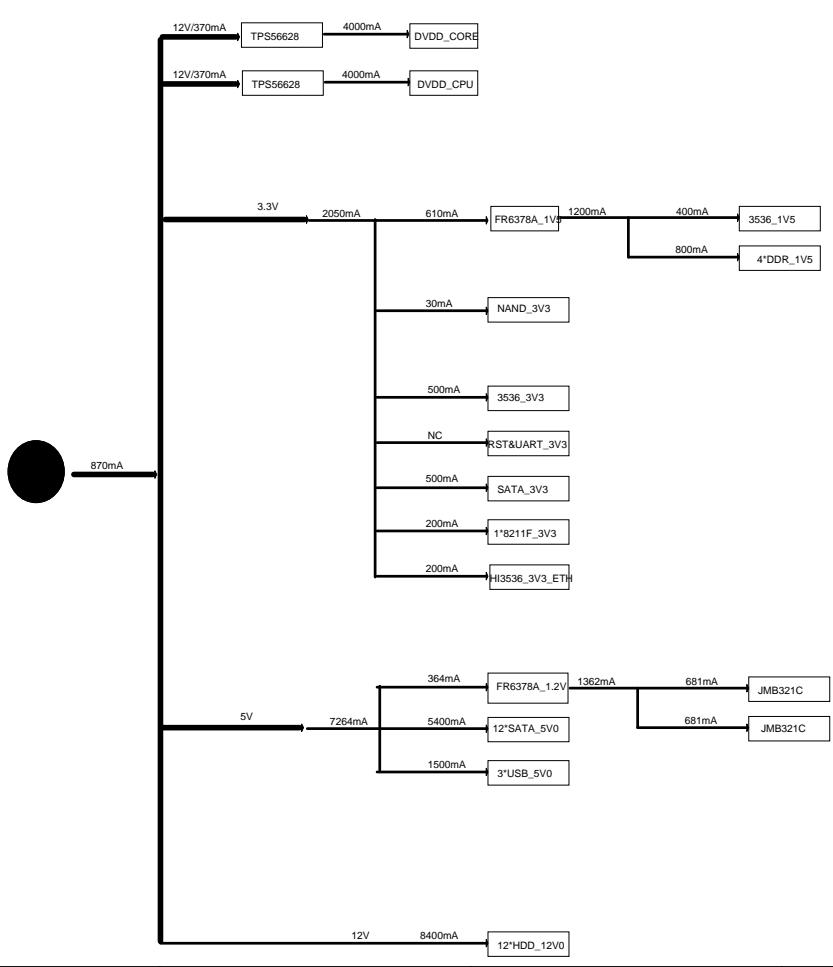


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POWER TREE

The adapter is at least 12VDO 7A adapter

5 4 3 2 1



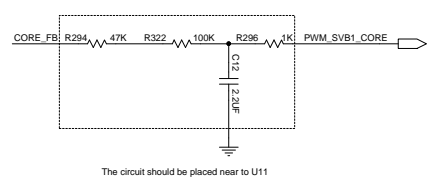
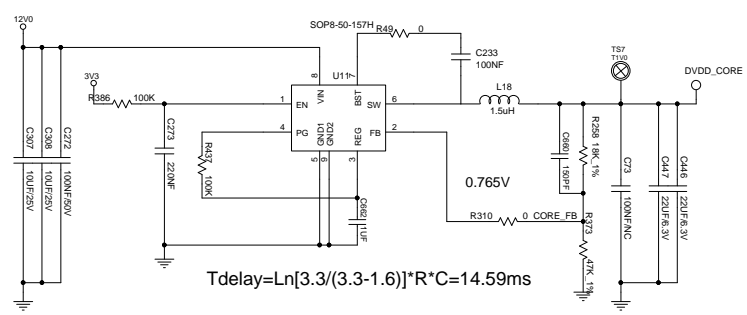
5 4 3 2 1

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5 4 3 2 1

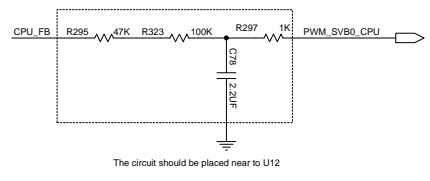
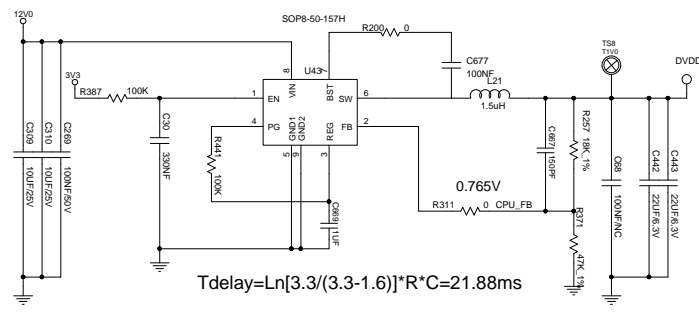
Power Supply

DC/DC 12V->DVDD_CORE 6Amax



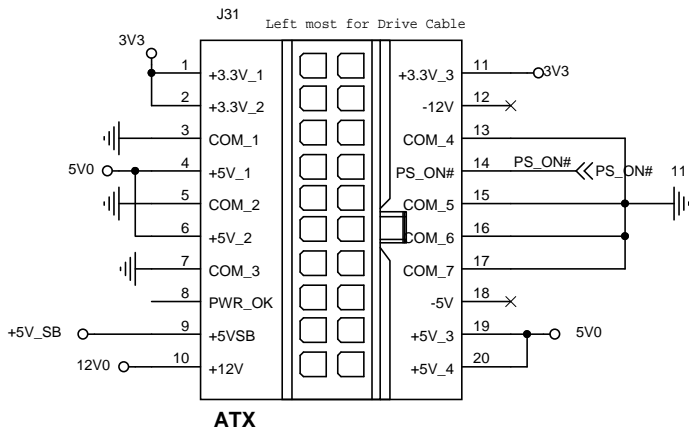
DC/DC 12V->DVDD_CPU 6Amax

SVB电阻的RC值见
《Hi3536硬件设计用户指南》P10 表 1-4 RC参数

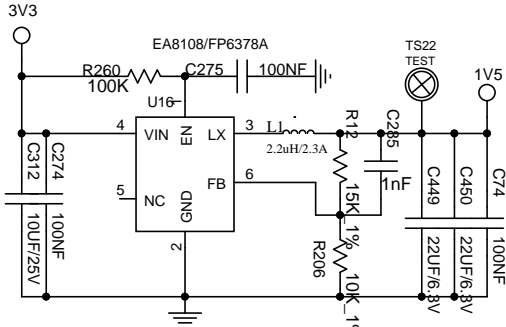


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Power Supply

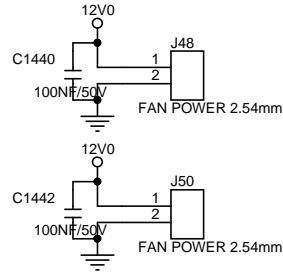
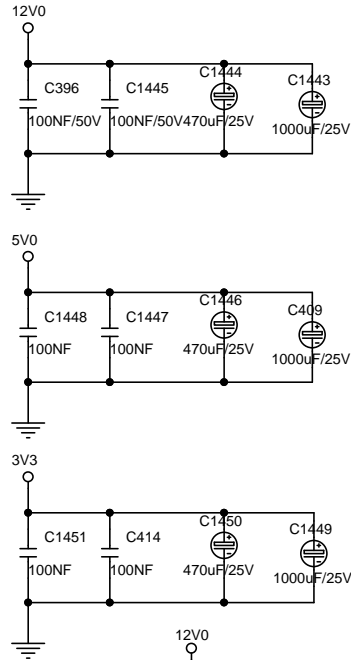


DC/DC 12V->1V5 1200Amax

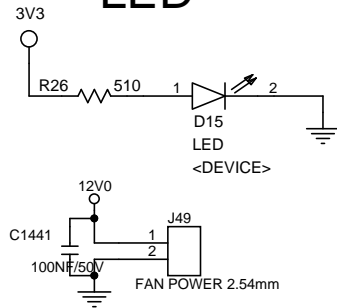


$$V_{out} = 0.6 * [1 + R_{12}/R_{206}] = 1.499V$$

$$T_{delay} = \ln[3.3/(3.3-2)] * R * C = 9.31ms$$

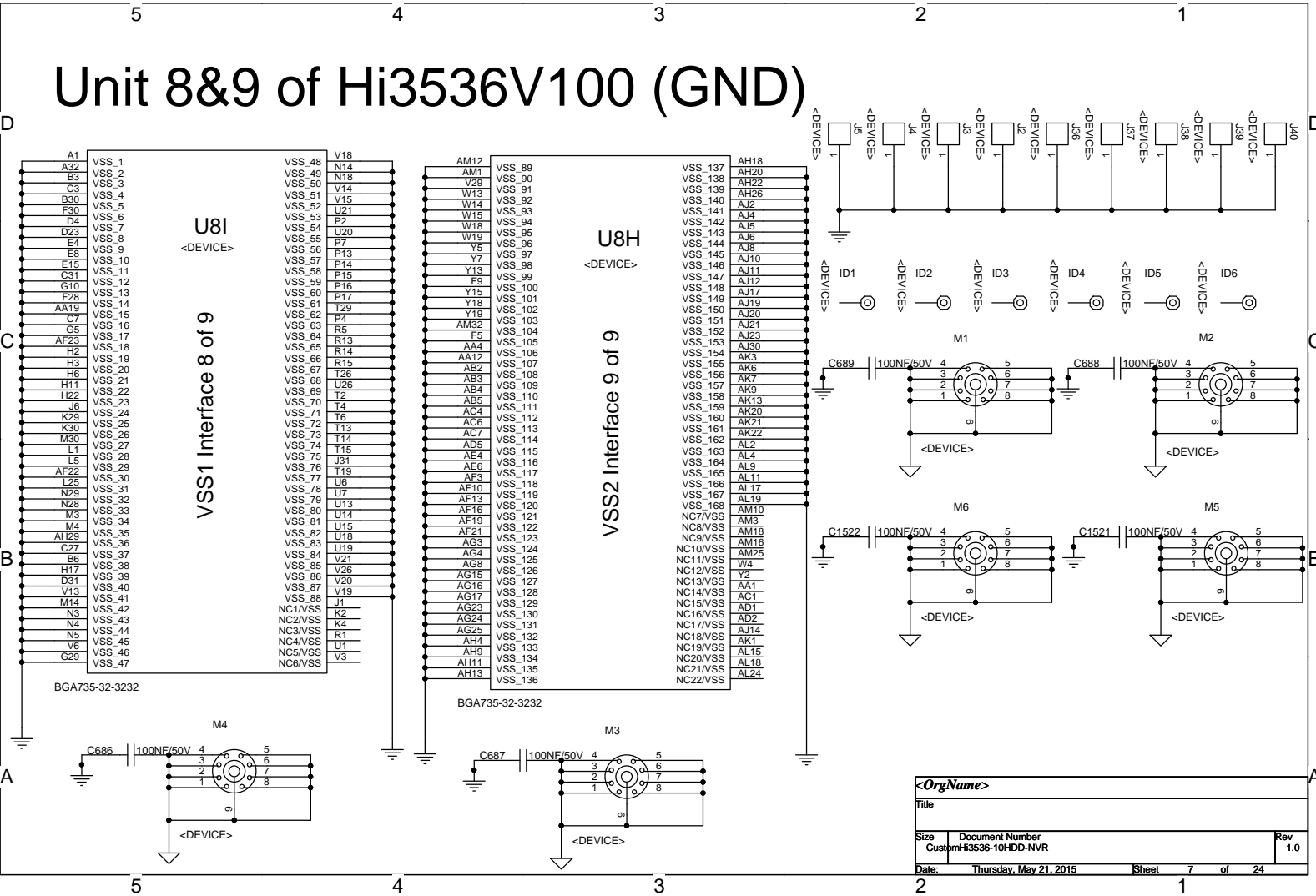


LED



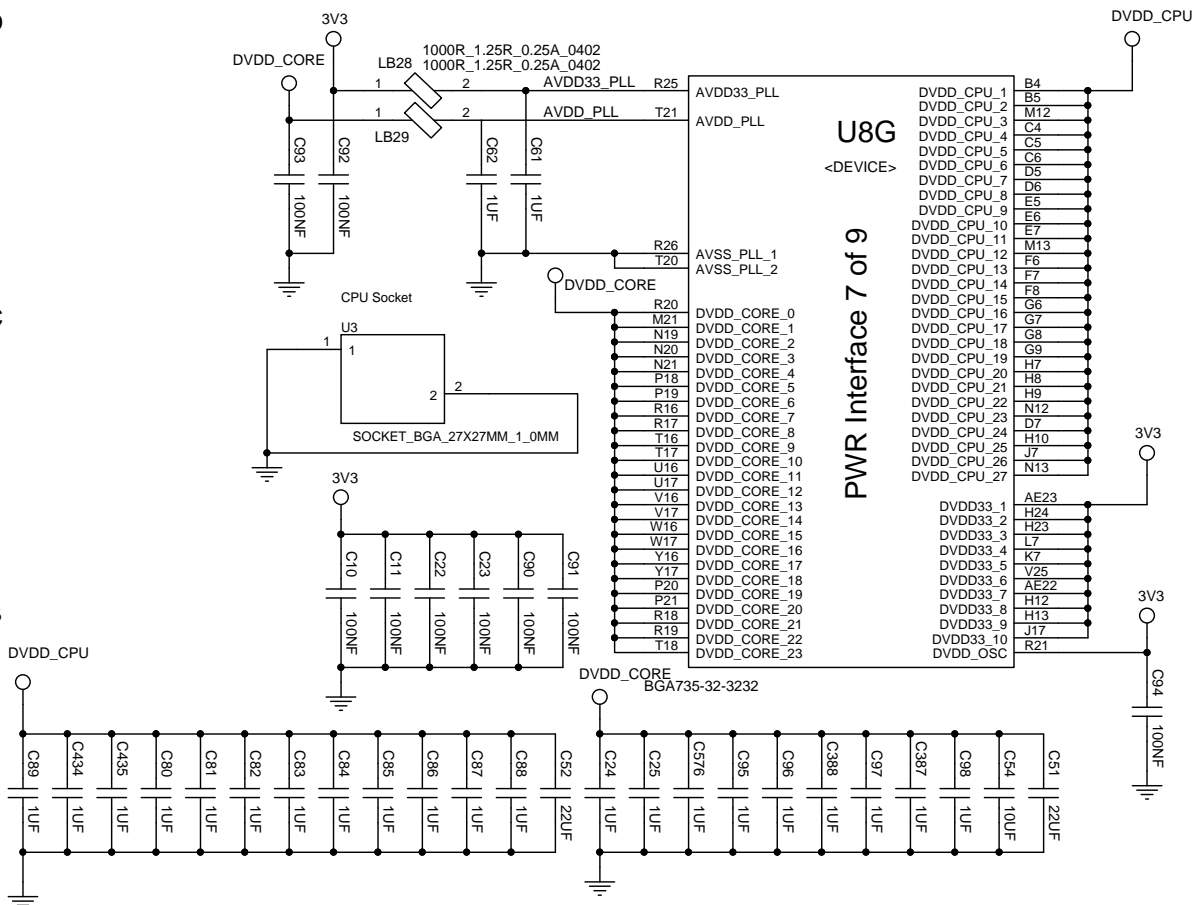
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Unit 8&9 of Hi3536V100 (GND)



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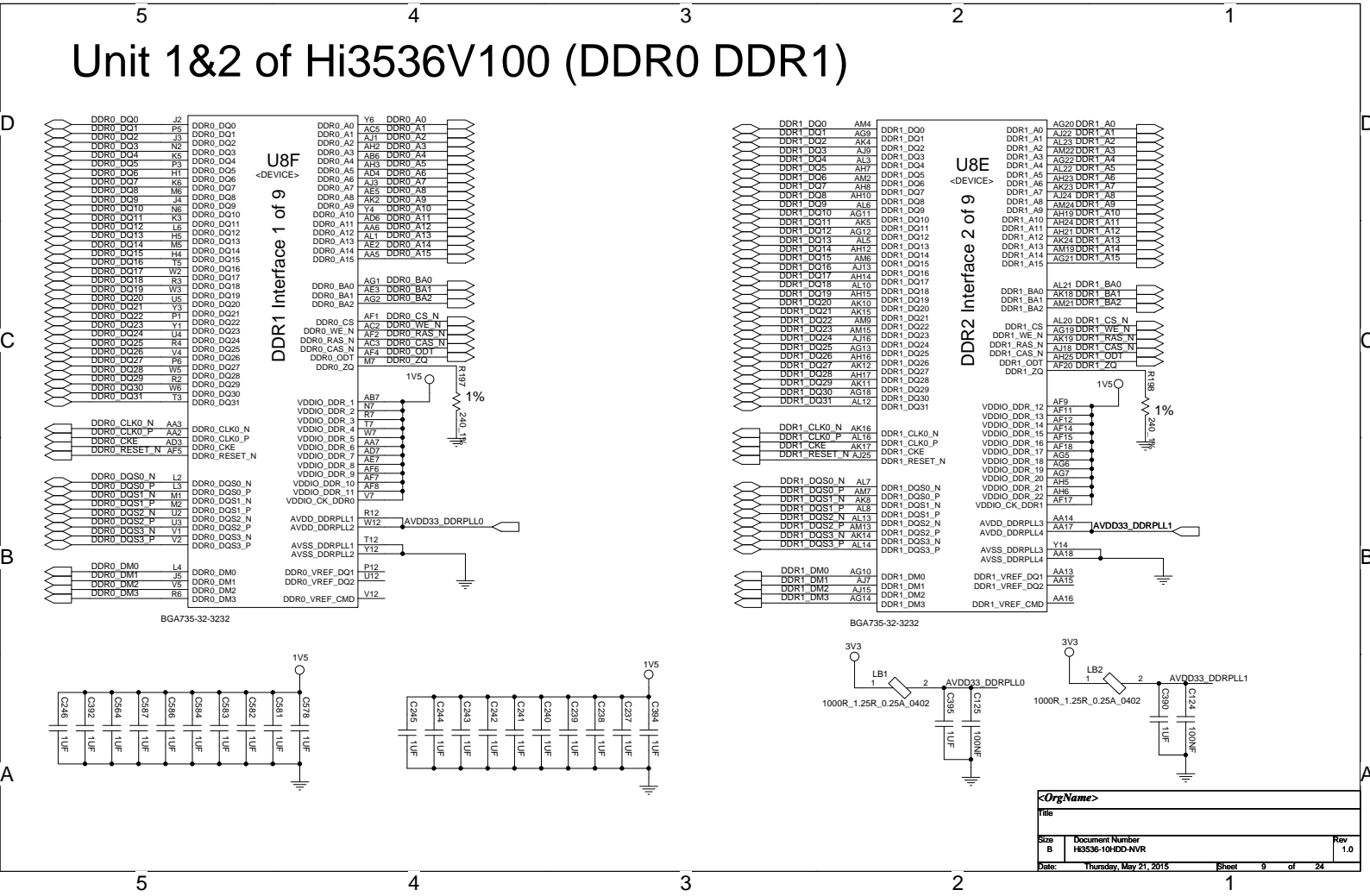
Unit 7 of Hi3536V100 (POWER)



The kind and quantity of the caps must be the same as that of Hi3536DMEB board

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Unit 1&2 of Hi3536V100 (DDR0 DDR1)

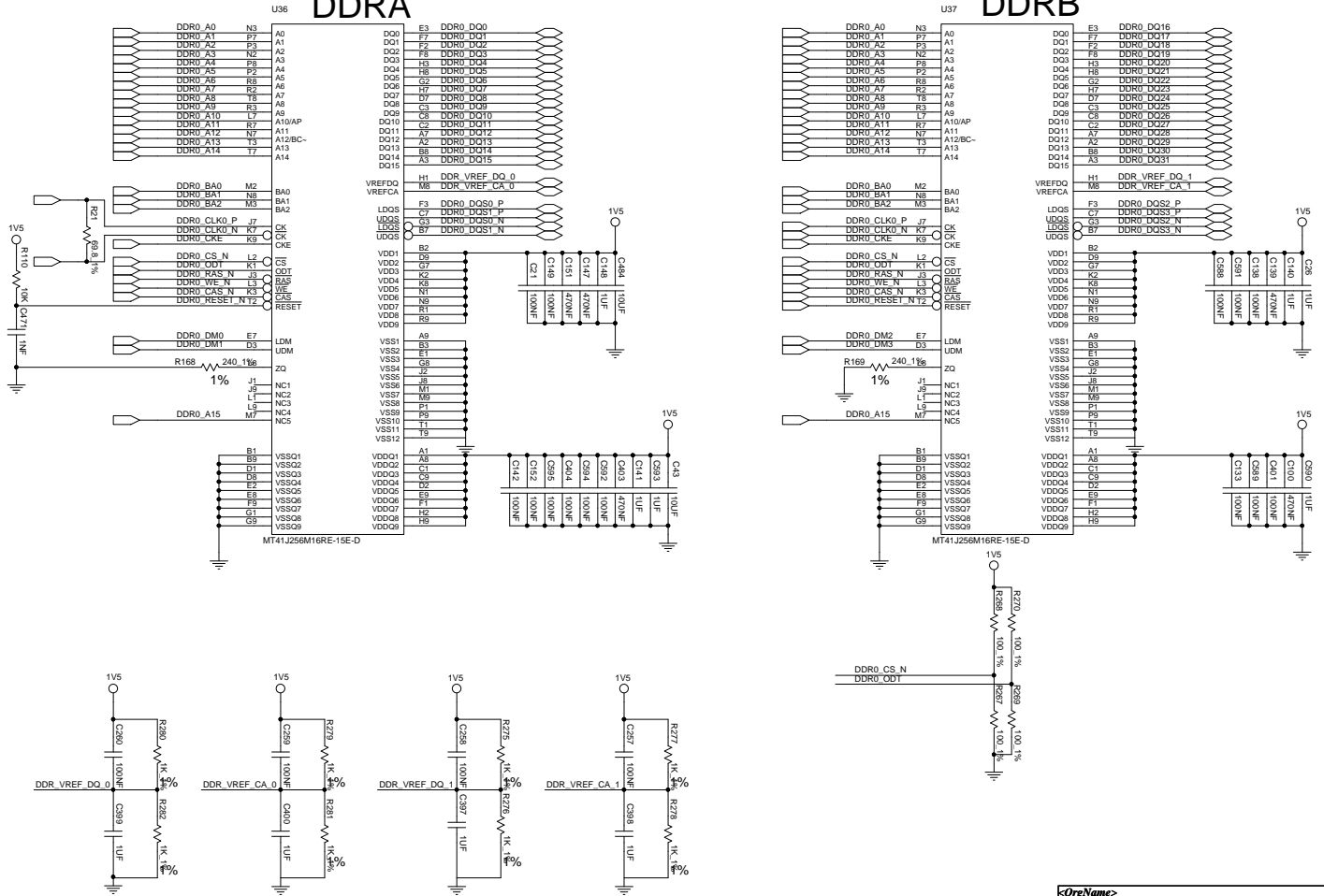


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DDRA&B NOVTT

DDRA

DDR B

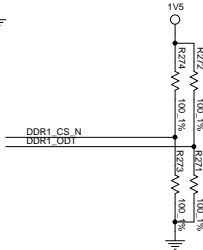
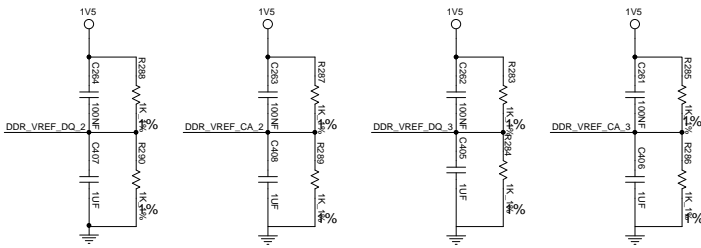
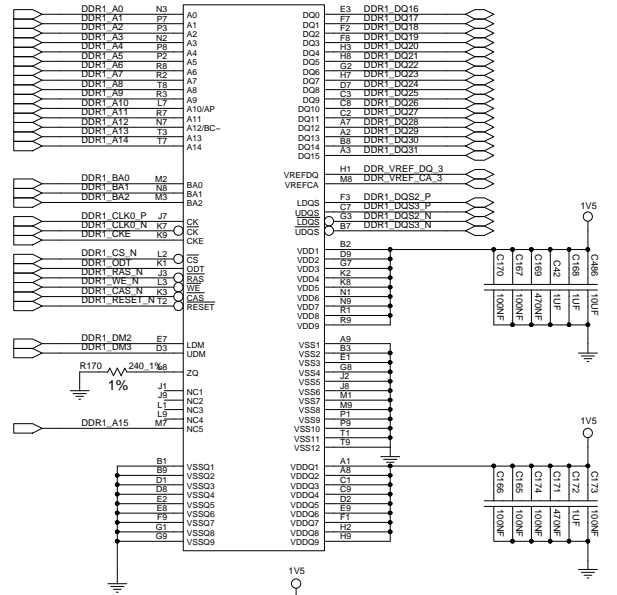
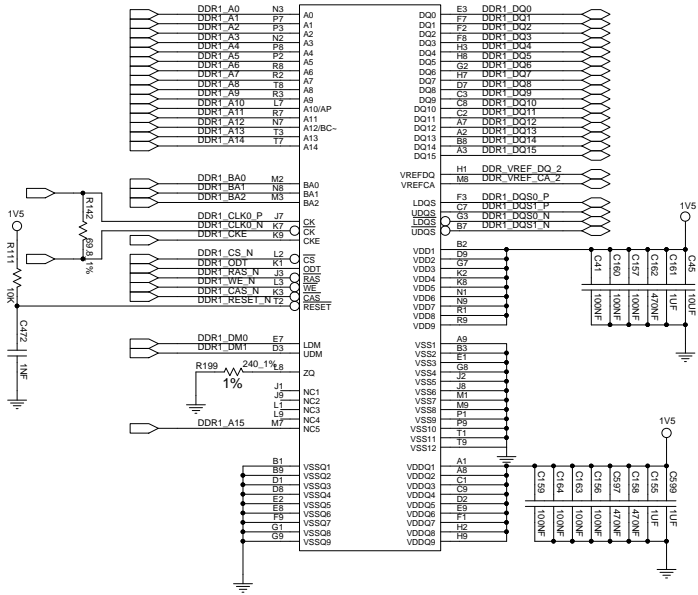


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DDRC&D NOVTT

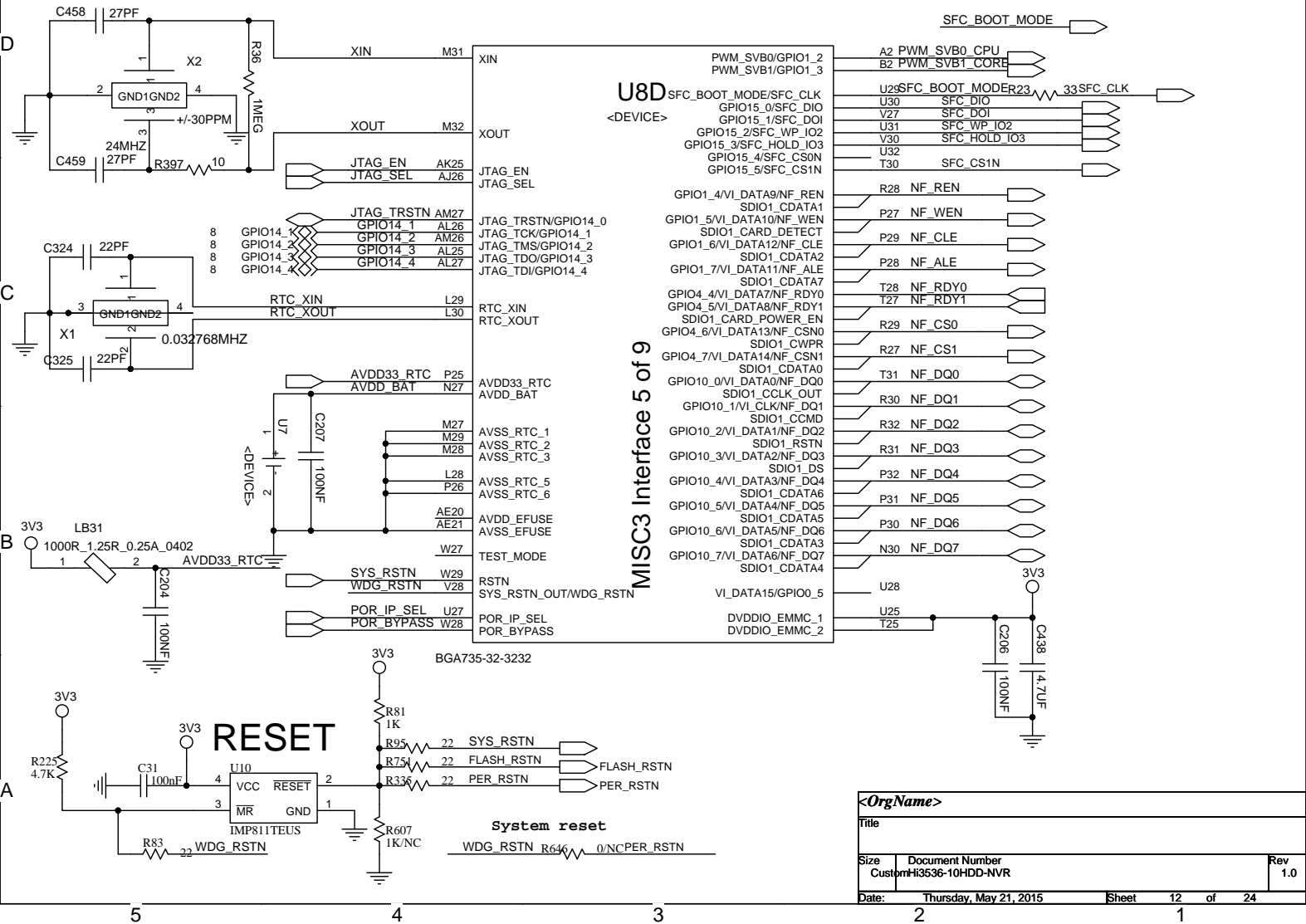
DDRC

DDR



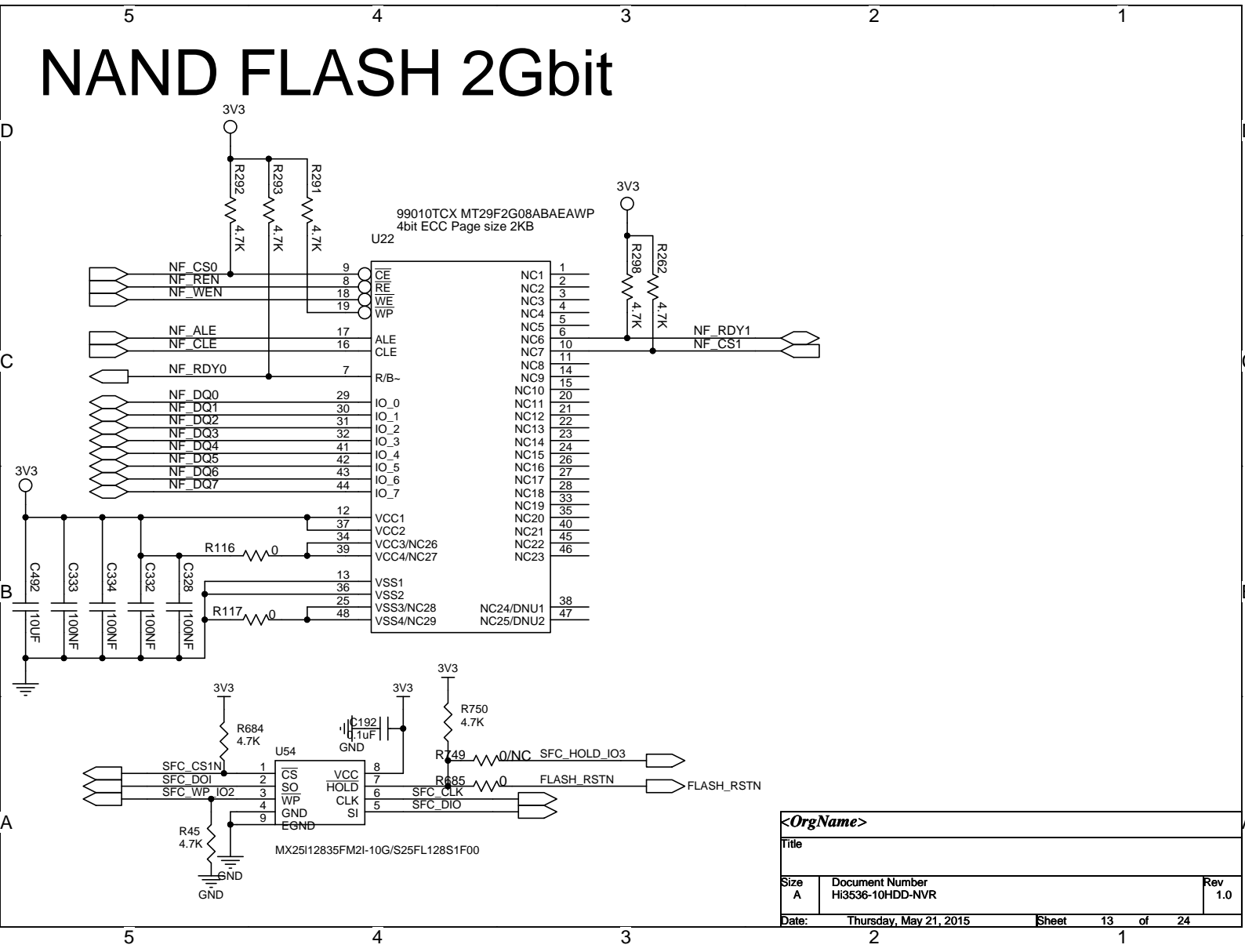
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Unit 5 of Hi3536V100 (SYSTEM)



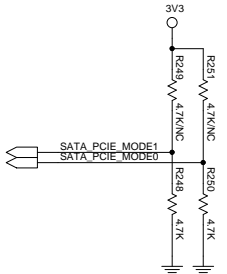
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NAND FLASH 2Gbit

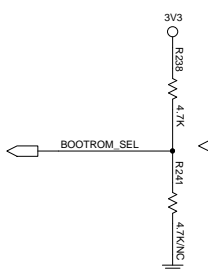


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2		1

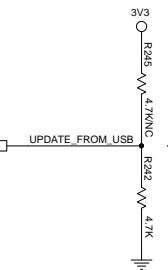
POWER ON SETTING



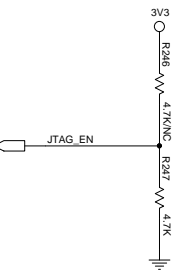
SATA PCIE_MODE1(0)	
00	4 Port SATA
01	3 Port SATA + PCIe X1
10	RESERVE
11	2 Port SATA + PCIe X2(default)



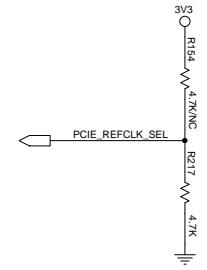
BOOTROM_SEL	
0	Boot from flash(default)
1	Bootrom Emmc/fastboot



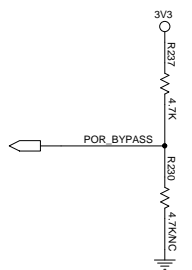
UPDATE FROM USB	
0	NOT UPDATE(default)
1	UPDATE FROM USB



JTAG_EN	
0	Disable JTAG(default)
1	Enable JTAG

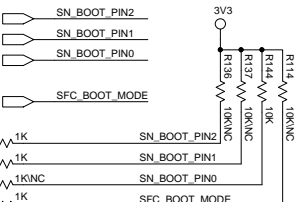


PCIE_REFCLK_SEL	
0	inter CRG clk(default)
1	external clk



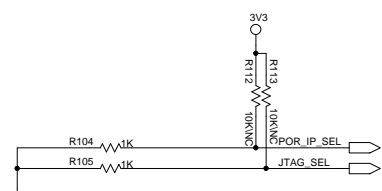
POR_BYPASS	
0	enable interior reset(default)
1	disable interior reset

4 PORT SATA



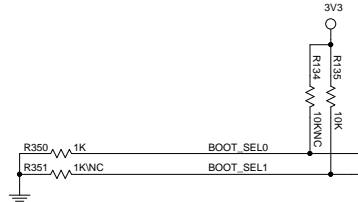
SF NAND_BOOT_PIN2		SFC_BOOT_MODE(SPI/Nand)	
0	2KB PageSize(default)	0	one line boot(default)
1	4KB PageSize	1	four line boot
SF NAND_BOOT_PIN1(0)		SFC_BOOT_MODE(SPI/NOR)	
00	RESERVE	0	3 Byte mode(default)
01	4bit ecc(default)	1	4 Byte mode
10	RESERVE		
11	24bit ecc		

2KB 4BIT ECC ONLY FOR SPI FLASH



JTAG_SEL	
0	Connect A17(default)
1	Connect A7
POR_IP_SEL	
0	Reset after Core power on(default)
1	Reset after IO power on

POR_BYPASS =1 POR_IP_SEL=0
3536 RESET BY RSTN PIN (811)

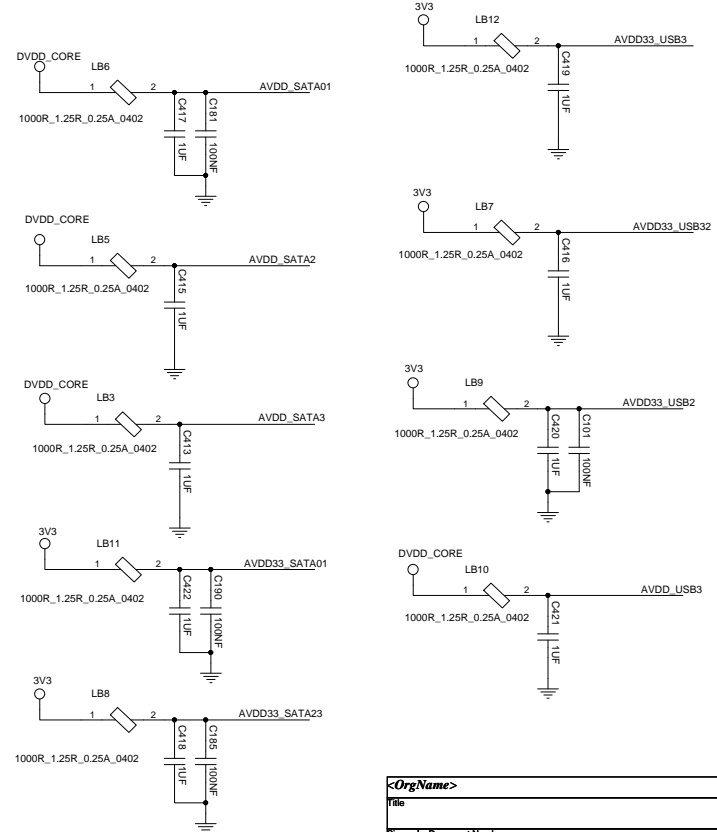
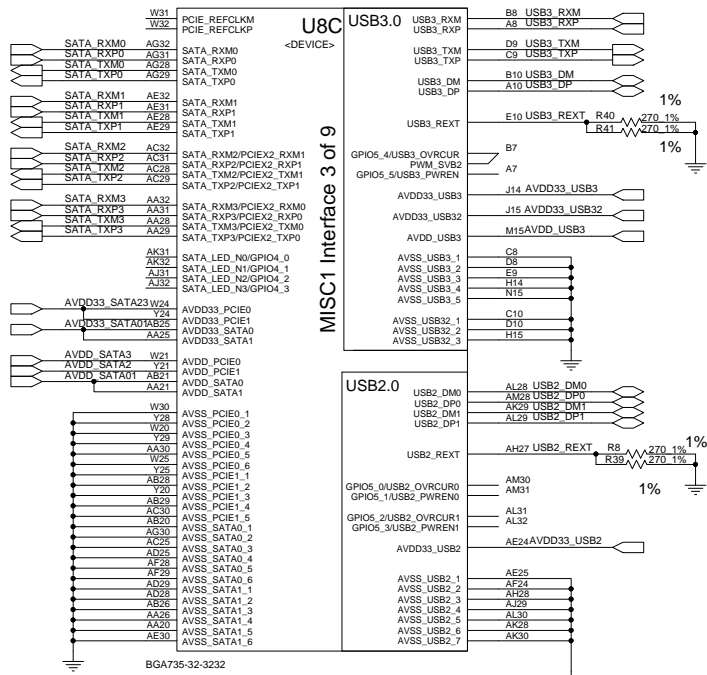


BOOT_SEL1(0)	
00	SPI NOR FLASH(default)
01	SPI NAND FLASH
11	SYSRAM

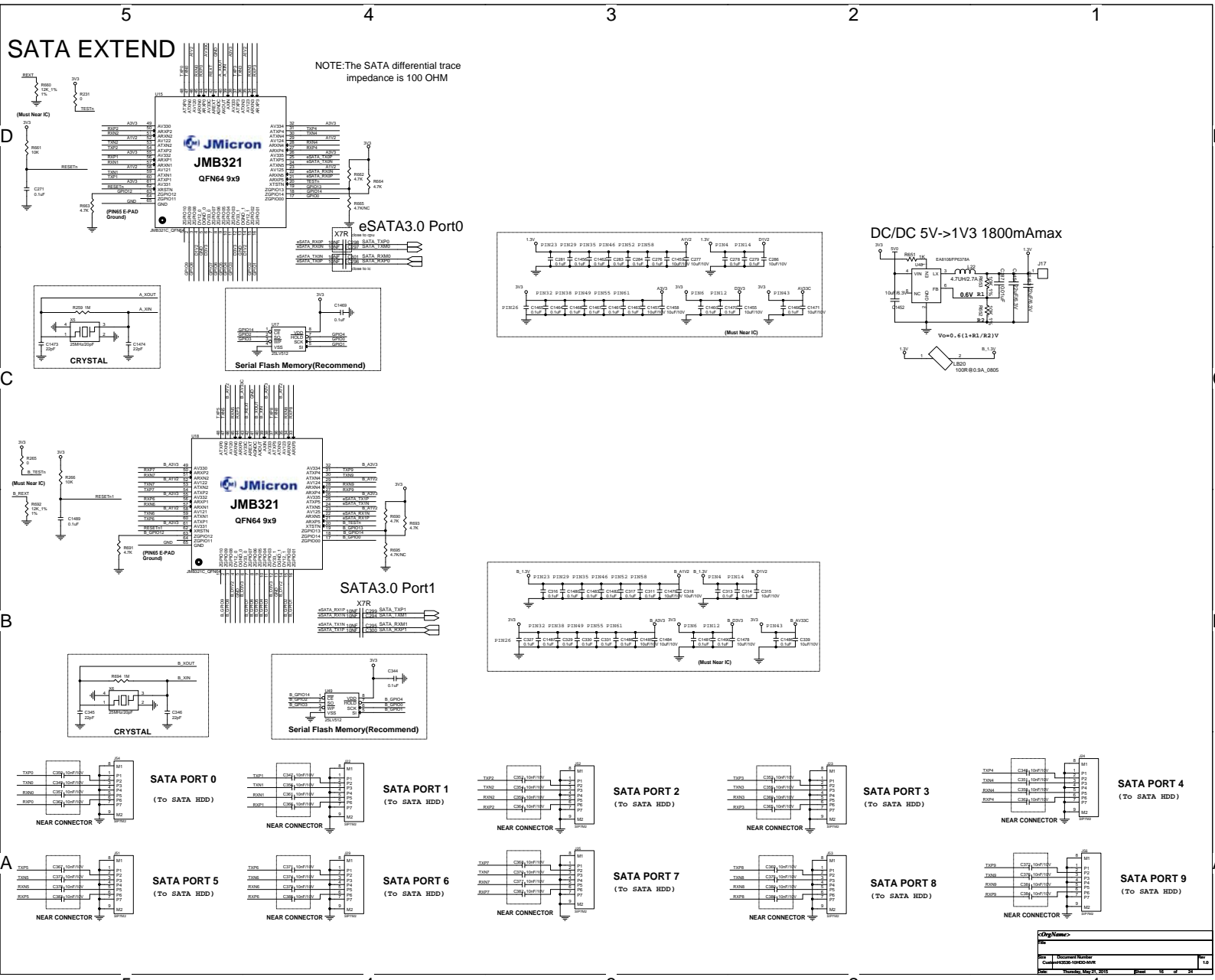
NAND FLASH

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Unit 3 of Hi3536V100 (INTERFACE0)

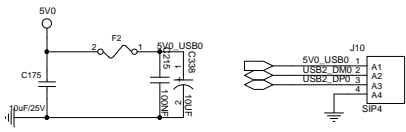


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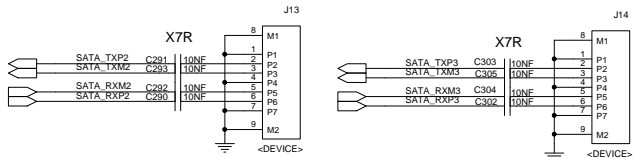


USB & SATA

USB2.0*1



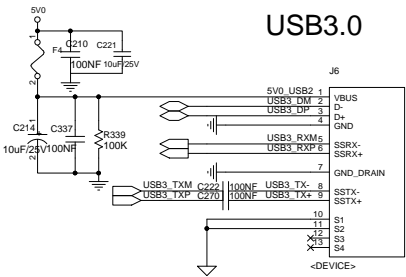
NOTES: The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.



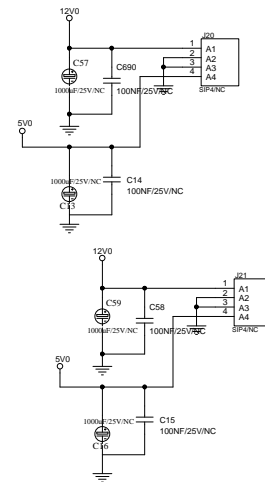
ESATA3.0 Port1

ESATA3.0 Port2

USB3.0

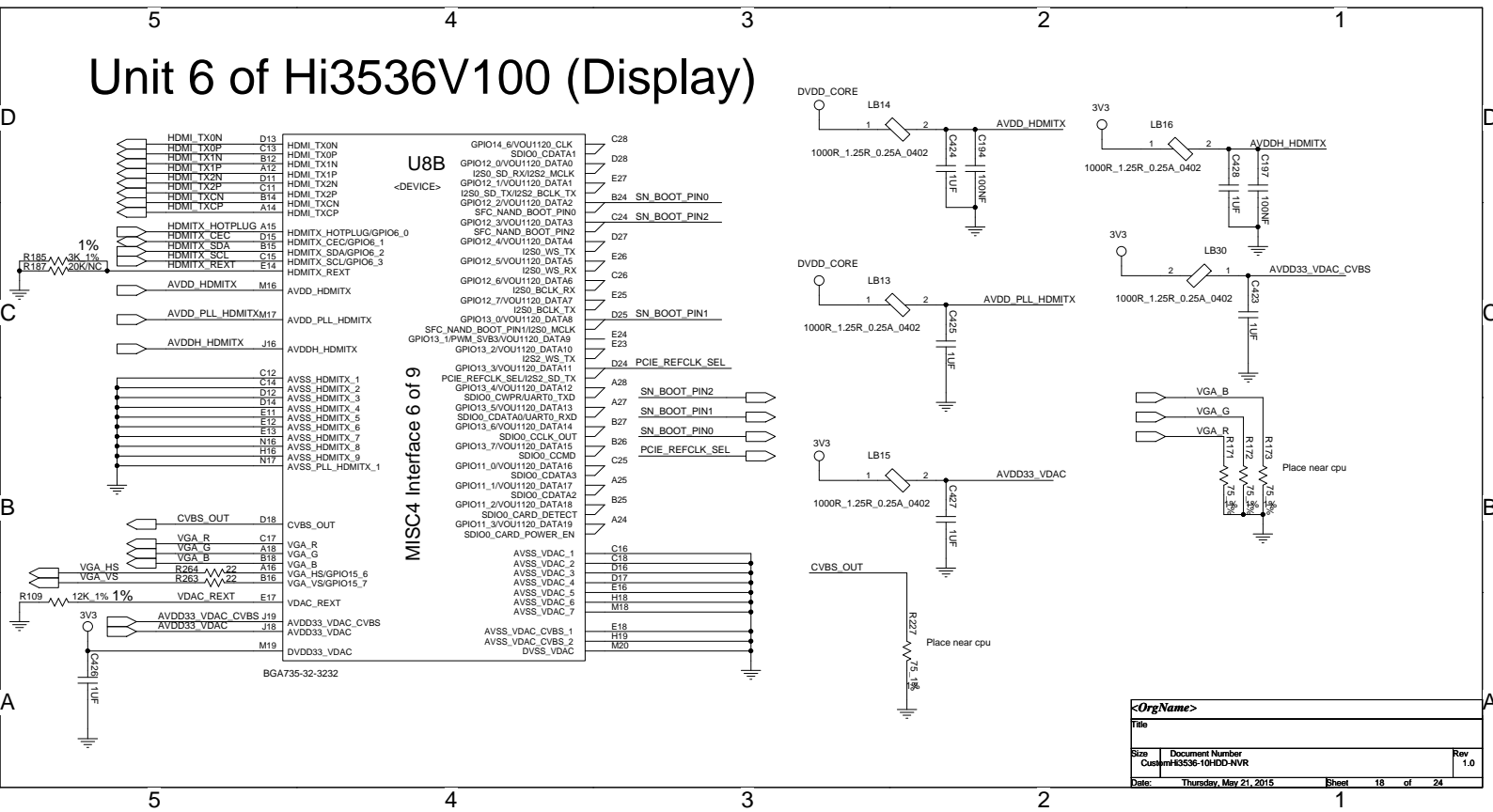


NOTES:
The USB differential trace impedance is 90 OHM.
The USB2.0 trace length is less than 8 inch.
The USB3.0 trace length is less than 5 inch.



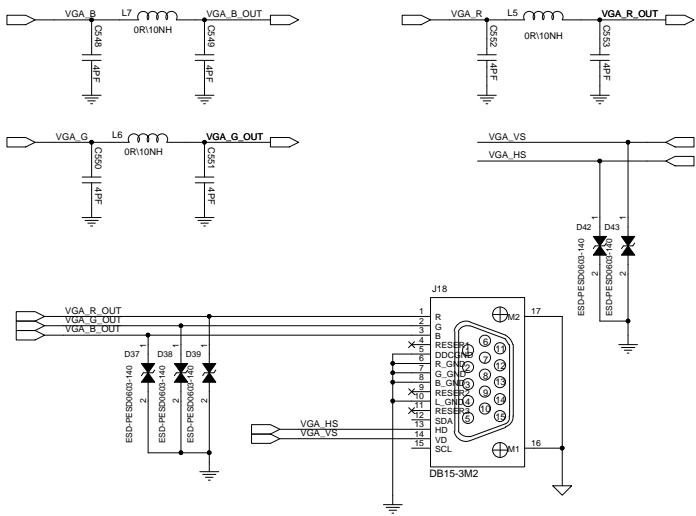
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Unit 6 of Hi3536V100 (Display)



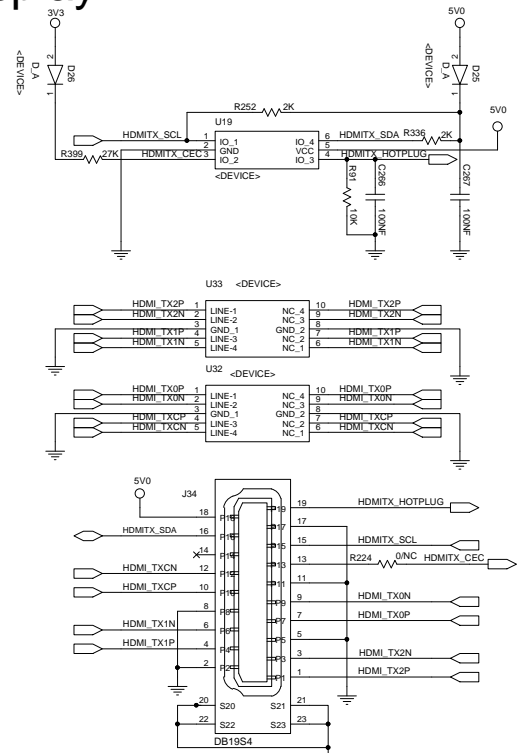
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Display VGA



NO CVBS OUTPUT

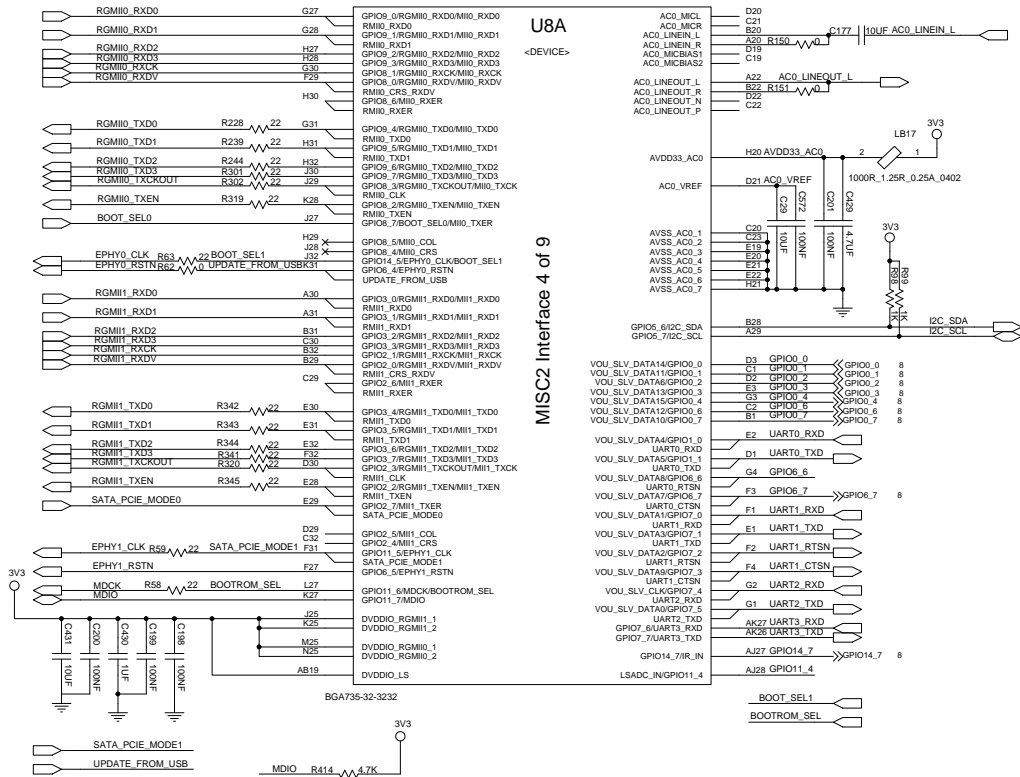
Display HDMI



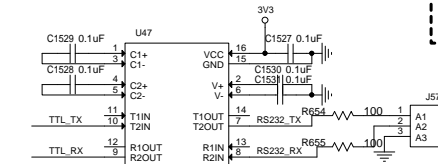
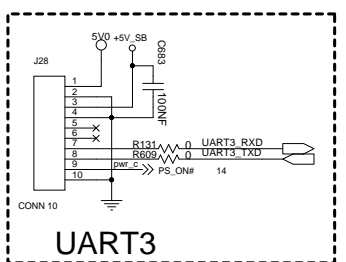
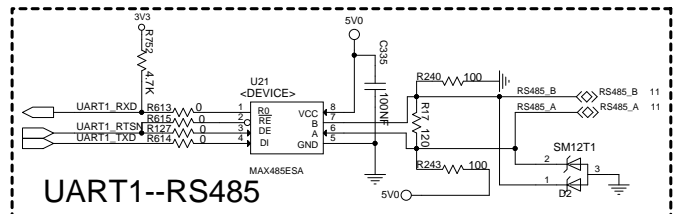
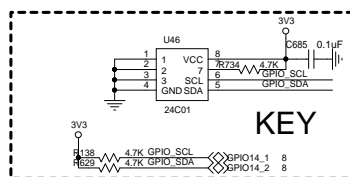
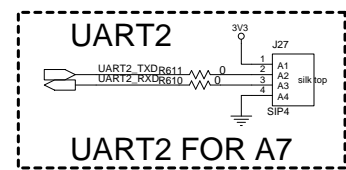
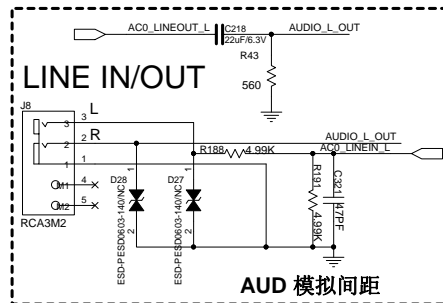
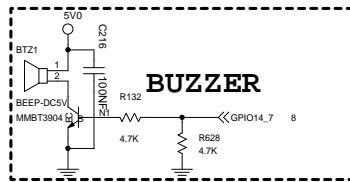
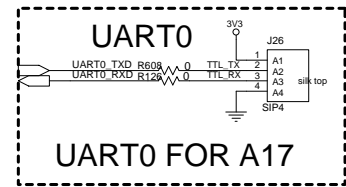
NOTES: The HDMI differential trace impedance is 100 OHM.
 The HDMI trace length is less than 5 inch.
 Pay attention to the junction capacitance of ESD component.
 We recommend that it be lower than 0.8pF

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Unit 4 of Hi3536V100 (INTERFACE1)

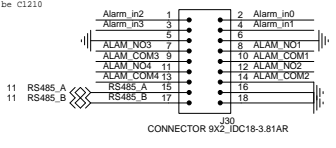
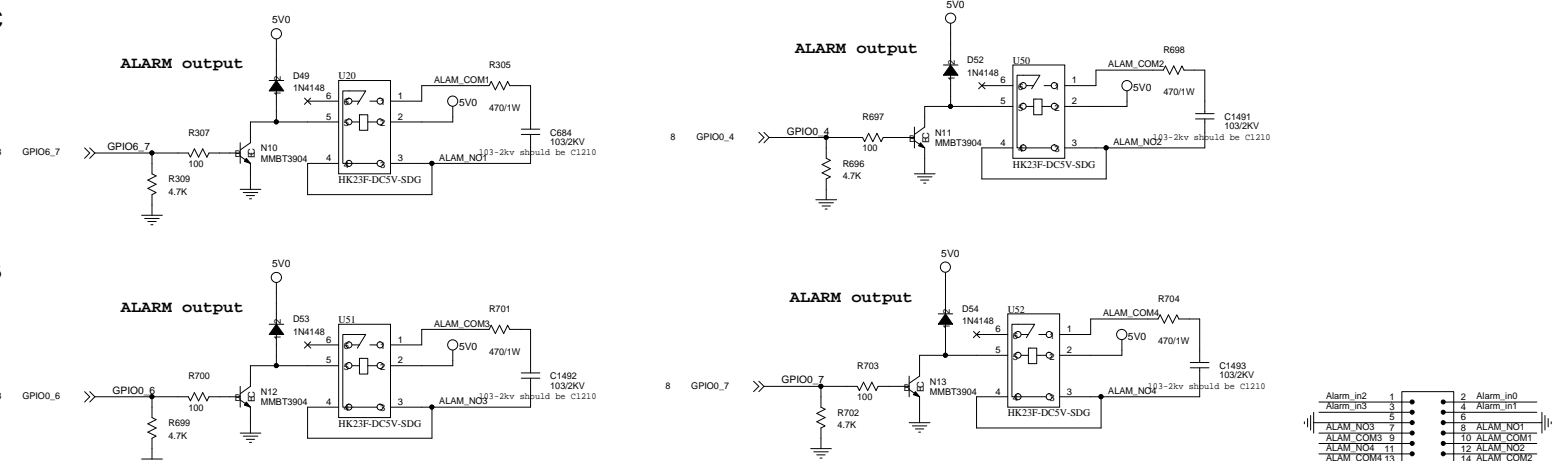
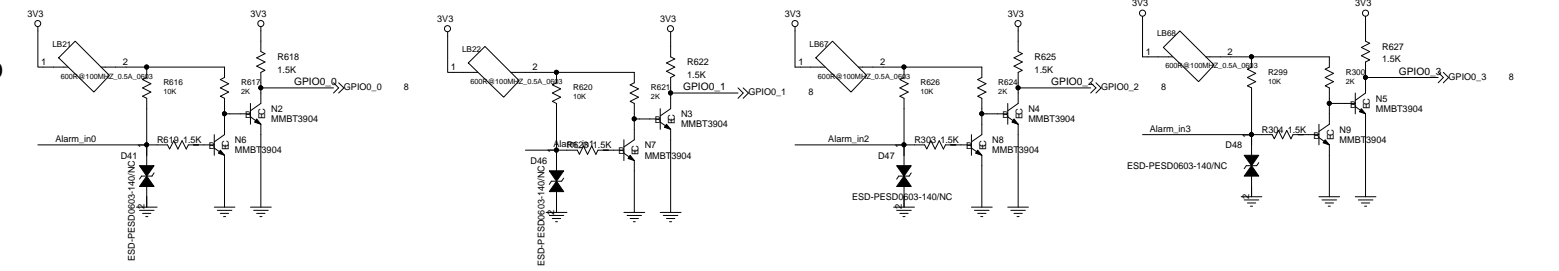


UART & RS485 & LINE IN/OUT & ALARM & KEY & BUZZER



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ALARM



Title		
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ETH0

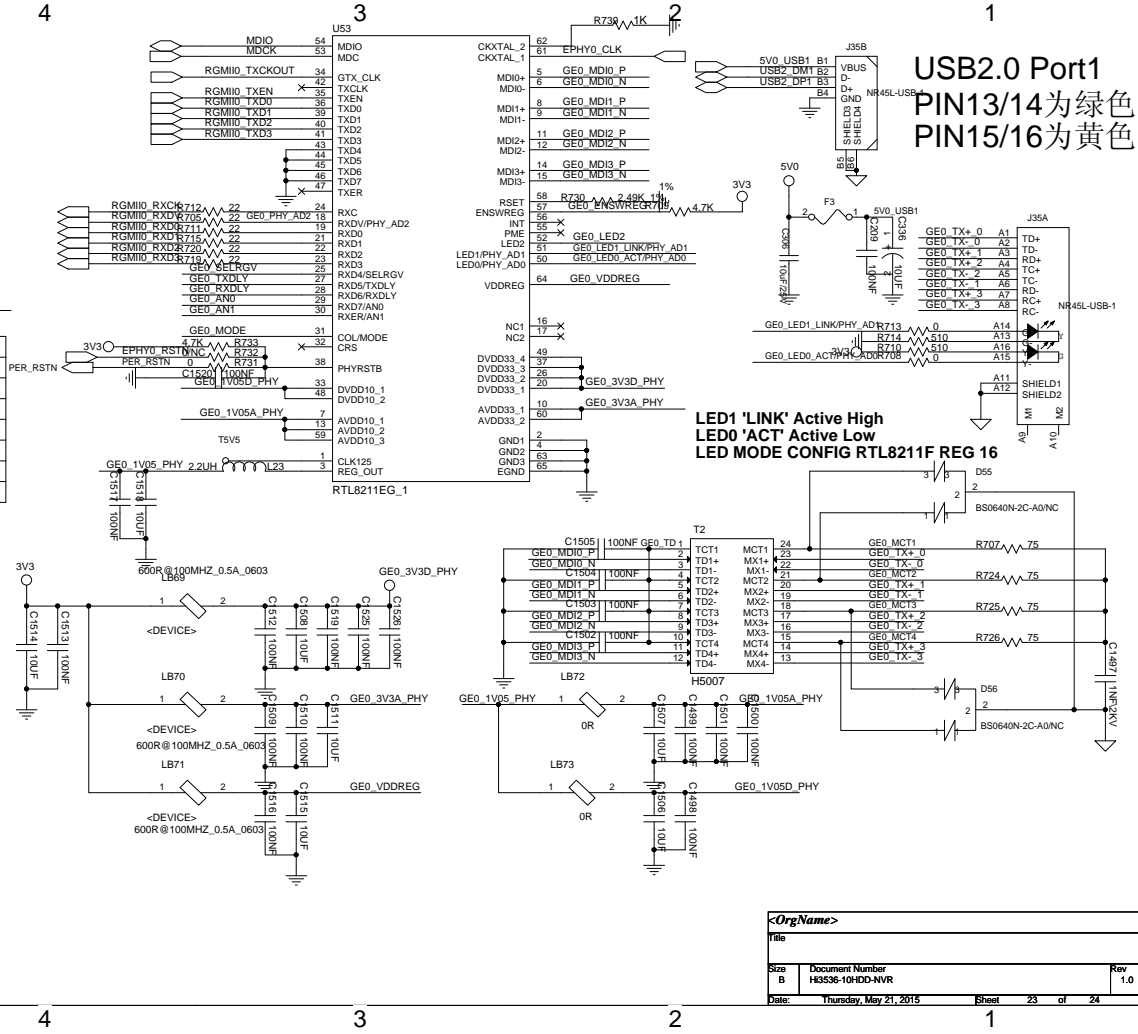
add 2ns delay to RXC/TXC for RXD/TXD latch
 Auto negotiation, advise all capabilities
 RTL8211EG_VB: Pull up for 3.3V
 1 = RGMII Mode

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
Internal 2.5V	1'b1	2'b11
Internal 1.8V	1'b0	2'b01
Internal 1.5V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

RGMII Power 设置为3.3V

与DEMO的PHY地址一致

PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111



ETH1

add 2ns delay to RXC/TXC for RXD/TXD latching

Auto negotiation, advise all capabilities
RTL8211EG_VB; Pull up for 3.3V
1 = RGMII Mode

GE1_3V3D_PHY

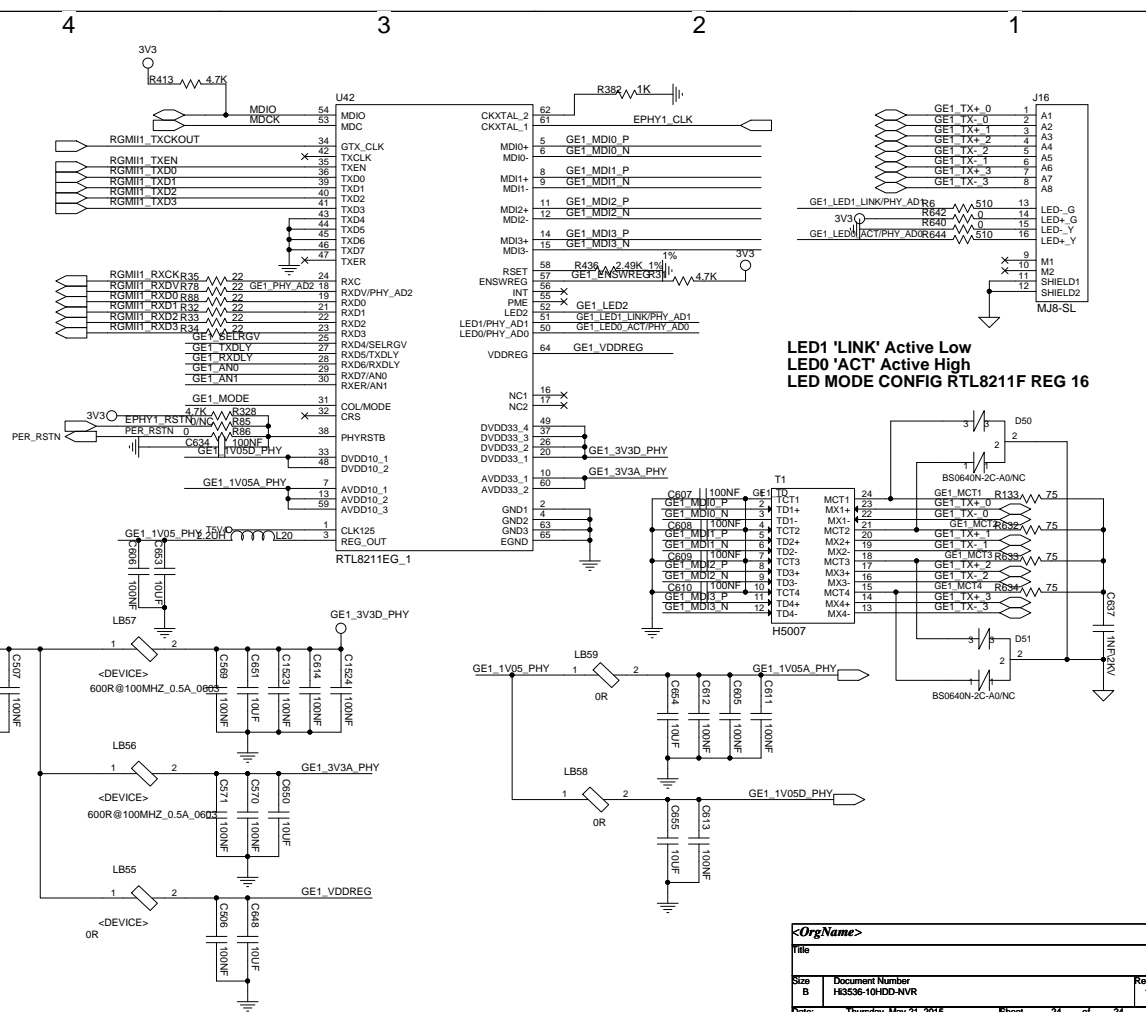
GE1_RXDLY R407 4.7K
GE1_TXDLY R408 4.7K
GE1_AND R412 4.7K
GE1_ANT R416 4.7K
GE1_SELRGV R725 4.7K
GE1_MODE R736 4.7K

GE1_3V3D_PHY

R411 4.7K GE1_LED0_ACT/PHY_AD0
R410 4.7K GE1_PHY_AD2

与DEMO的PHY地址一致

PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111



LED1 'LINK' Active Low
LED0 'ACT' Active High
LED MODE CONFIG RTL8211F REG 16

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